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UNIVERSITY OF ALBERTA

INVESTIGATION OF JUNCTION TEMPERATURE EFFECTS ON AN RF POWER AMPLIFIER MODEL

BY

BLAIR MELVIN CAIN

(C)

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE.**

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

FALL 1991

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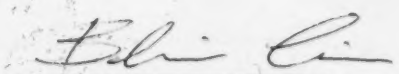

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To my parents and sister,

For their love, support, and encouragement over the years.

ABSTRACT

This thesis investigates the use of a temperature-dependent RF bipolar transistor model to predict the response of an RF power amplifier. The model is intended for cellular radio applications, in which the system components are specified to operate over wide ambient temperature and output power ranges. Transistors in these systems experience large junction temperature variations due to variable heatsink temperatures and self-heating.

The transistor model is based on the Gummel-Poon charge control model. This model describes both linear and non-linear device behavior, and its parameters are determined from DC and small-signal terminal measurements. Package parasitics are represented by an equivalent lumped-element network and are optimized to correspond to small-signal S-parameter measurements.

The transistor model is used to predict the performance of an experimental 850 MHz class B amplifier. The amplifier's input and output matching networks are characterized using small-signal measurements and optimization techniques. An electrical temperature measurement technique is developed for the RF transistor operating in the class B amplifier, to avoid inaccuracies associated with a thermal resistance model.

The transistor and amplifier models are combined with the measured temperature data to simulate the experimental amplifier. The complex device structure makes it difficult to determine an accurate transistor model prior to building the experimental circuit. Accurate simulation results are achieved by adjusting the parasitic network element values and various model parameters, after the experimental amplifier performance has been determined. The final model predicts output powers which are within 0.5 dB of measured over an

input power range of 28 to 33 dBm. The modeled DC collector current is within 10% of measured over this same input power range. The results indicate that while several model parameters are strong functions of junction temperature, the performance of the transistor is largely determined by the effects of the package parasitics.

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LIST OF SYMBOLS

A	Emitter cross-sectional area
β_F	Forward current gain
β_R	Reverse current gain
C_{jc}	Zero-bias base-collector junction capacitance
C_{je}	Zero-bias base-emitter junction capacitance
C_μ	Small-signal hybrid-π base-collector capacitance
C_π	Small-signal hybrid-π base-emitter capacitance
D_n	Diffusion constant for electrons
D_p	Diffusion constant for holes
ε_r	Relative permittivity
E	Electric field
E_g	Energy gap for silicon
ϕ_C	Base-collector built-in potential
ϕ_E	Base-emitter built-in potential
f_T	Unity gain bandwidth
γ	Propagation constant
η_{CL}	Base-collector leakage emission coefficient
η_{EL}	Base-emitter leakage emission coefficient
η_F	Forward current emission coefficient
η_R	Reverse current emission coefficient
I_C	Collector current
I_{CT}	Generator current in the hybrid-π model
I_K	Forward knee current
I_{KR}	Reverse knee current
I_S	Saturation current

I_{SC}	Base-collector leakage saturation current
I_{SE}	Base-emitter leakage saturation current
I_{SS}	Zero-bias saturation current
J_n	Diffusion current density due to electrons
J_p	Diffusion current density due to holes
m_c	Base-collector junction grading coefficient
m_e	Base-emitter junction grading coefficient
n	Free electron concentration
n_i^2	Intrinsic carrier concentration
N_A	Doping density in p-type material
N_D	Doping density in n-type material
μ_n	Electron mobility
μ_p	Hole mobility
p	Hole concentration
P_{in}	Input RF power
P_{out}	Output RF power
q	Electronic charge
q_b	Normalized total majority charge in the base
q_C	Increased majority charge in the base due to base-collector basewidth modulation (normalized)
q_E	Increased majority charge in the base due to base-emitter basewidth modulation (normalized)
q_F	Excess majority charge in the base due to base-emitter bias voltage (normalized)
q_R	Excess majority charge in the base due to base-collector bias voltage (normalized)
q_1	Basewidth modulation component of q_b
q_2	High-level injection component of q_b

Q	Quality factor
Q_B	Total majority charge in the base
Q_{BO}	Zero-bias total majority charge in the base
Q_C	Increased majority charge in the base due to base-collector basewidth modulation
Q_E	Increased majority charge in the base due to base-emitter basewidth modulation
Q_F	Excess majority charge in the base due to base-emitter bias voltage
Q_R	Excess majority charge in the base due to base-collector bias voltage
r_b	Base resistance
r_c	Collector resistance
r_e	Emitter resistance
r_π	Small-signal hybrid-π base-emitter resistance
r_o	Small-signal hybrid-π output resistance
R_θ	Thermal resistance
τ_B	Forward base transit time
τ_{BR}	Reverse base transit time
τ_F	Total forward transit time
τ_{FR}	Total reverse transit time
T_j	Junction temperature
V_A	Forward Early voltage
V_B	Reverse Early voltage
V_K	Forward knee voltage
V_{KR}	Reverse knee voltage
W_B	Basewidth
x_c	Collector side of the collector-base depletion region

$x_{co'}$	Zero-bias value of $x_{c'}$
$x_{e'}$	Emitter side of the emitter-base depletion region
$x_{eo'}$	Zero-bias value of $x_{e'}$
Z_o	Characteristic impedance

LIST OF ABBREVIATIONS

AC	Alternating Current
BJT	Bipolar Junction Transistor
CAD	Computer-aided Design
CW	Continuous Wave
DC	Direct Current
E-M	Ebers-Moll
FM	Frequency Modulation
FET	Field Effect Transistor
GaAs	Gallium Arsenide
G-P	Gummel-Poon
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
PF	Performance Function
PM	Phase Modulation
RF	Radio Frequency
RFC	Radio Frequency Choke
TDMA	Time Division Multiple Access
TSEP	Temperature Sensitive Electrical Parameter

1. INTRODUCTION

Non-linear circuit simulation is an important tool for designing and optimizing radio frequency (RF) power amplifiers (PAs). The conventional approach to the design of RF PAs has been largely experimental; a prototype is built based on a simplified design and then modified semi-empirically until it meets the design specifications.

In addition to reducing development time and costs, the incorporation of simulation in the design phase provides several advantages over the prototyping method [1]. Computer-aided analysis enables the designer to conveniently investigate the effects of variable device parameters and environmental conditions. As well, ideal probes may be used to observe voltage and current waveforms at locations which would normally be difficult or impossible to access on the actual circuit. By analyzing the simulation results, the designer can obtain an increased understanding of the circuit's operation and potential problem areas, so that it is less likely that significant design changes will be necessary when the circuit is built.

Although circuit simulation offers several advantages over conventional design approaches, its use in the design of RF PAs has been limited. This is mainly a result of the complex transistor models which must be used in order to obtain the required degree of accuracy for RF circuit design [2]. This is particularly true for class B and C amplifier design, where the transistor model must be accurate over several regions of operation. Hence, the primary advantage of reduced development time and cost using simulation is often offset by the significant time and effort necessary to develop accurate transistor models.

Difficulties in developing relatively simple yet accurate non-linear transistor models have inhibited the widespread use of simulation in the design of RF PAs. Instead, it has been more convenient to use adjustable components and experimental optimization of the amplifier. However, an increased demand for miniaturization in wireless communication equipment, such as portable cellular telephones, necessitates the use of miniaturized circuits with reduced tuning capabilities. The use of miniature circuits and monolithic microwave integrated circuits (MMICs) is not only desirable to reduce product size, but also to increase reliability and reduce manufacturing costs. The conventional prototyping approach is impractical for the development of these specialized RF circuits for several reasons [3]:

1. Physical circuit dimensions are not negligible with respect to wavelength at high frequencies. Hence, the design of a prototype which is truly equivalent to the MMIC or hybrid implementation is difficult.

2. Parasitics are very significant at RF, causing the expected behavior of the devices to be significantly different from that of the discrete prototype.

3. Using an "experimental" technique, in which a design evolves from successive measurements made on prototype MMICs, is very inefficient. In addition to the high cost of making prototype MMICs in small quantities, accurate testing is difficult. This is especially true for an RF circuit, for which it is difficult to make measurements without significantly altering the circuit's operation. Hence, test results do not always identify exactly how the design should be changed to obtain the desired performance.

As outlined above, the need for miniature RF circuits in wireless communication systems has led to a change in the role of simulation from an optional design aid to an essential design tool. In addition to assisting in the design of RF semiconductors, there is increasing interest in the use of simulation to characterize the performance of discrete RF PAs in cellular radio transmitters. Active device temperature is an important parameter for this application since the PA is specified to operate over a wide ambient temperature range (-30 to +60 °C [4]). Also, as a transmitter moves within a cell, the cellsite instructs the transmitter to change its output power level (-22 to +6 dBW nominal effective radiated power for a class I mobile station transmitter [4]) in order to maintain a constant received power level at the base station. This in turn causes variations in the PA's internally dissipated power, and hence, the junction temperature of the active device due to self-heating. Finally, temperature is important for system components in the upcoming digital cellular radio network. The proposed format for the time division multiple access (TDMA) multiplexing scheme includes a 20 ms frame with a transmit duty cycle of 33% [4]. This signal specification necessitates a model which includes dynamic temperature changes since the transmit times are of the same order as the active device's thermal time constant (unlike low duty cycle applications such as pulsed radar).

The aim of the research reported in this thesis is to determine the importance of temperature as a design parameter for cellular radio transmitters by investigating the effect of junction temperature on RF power transistor performance. Specifically, junction temperature effects are investigated for RF bipolar junction transistors (BJTs). The use of silicon BJTs is very attractive for cellular radio applications since their cost is much less than that of GaAs FET devices offering similar performance.

1.1 RF Simulation Techniques

A significant amount of effort has gone into the development of analysis techniques for the simulation of non-linear circuits [5]. A number of approaches have been formulated and are usually distinguished by the way in which linear and non-linear circuit elements are treated.

1.1.1 Large-signal S-parameter Technique

The large-signal S-parameter technique analyses microwave circuits in the frequency domain. Each non-linear device is represented by an equivalent two-port network which is characterized by a set of S-parameters. Although the use of S-parameters assumes a strictly linear network, they have been used to characterize large-signal transistor behavior [6,7]. Transistor operation is inherently non-linear in a large-signal amplifier, since during a single RF cycle the transistor operates in the cutoff, saturation, and forward active regions. The use of S-parameters is justified by the observation that the terminal voltages of a transistor operating as a class C amplifier are nearly sinusoidal, due to the effect of the package parasitics [8].

The primary advantage of this method is that simulation of the linearized circuit is very efficient. As well, useful S-parameter techniques developed for the design of small-signal amplifiers may be used for large-signal design.

This method is not often employed, since the measurement of large-signal S-parameters is time consuming. To obtain reasonably accurate results, measurements must be made under conditions very close to the actual amplifier operating conditions. This normally requires a high-power RF source, since RF BJTs have high reflection coefficients in a standard 50 or 75 Ω measurement system. As well, S-parameters depend on drive level and bias

conditions, and an accurate characterization requires measured data over the various operating regions in which the transistor is expected to operate.

Assuming accurate S-parameter data are available, this method does not provide the necessary accuracy for the previously discussed simulation requirements. Linearization of the amplifier immediately causes inaccuracies and limits the applicability of the analysis to mildly non-linear amplifiers. While this may be acceptable for amplifiers operating close to the f_t of the transistor, this is not the case for the amplifier used in this project. In addition, load line dependent characteristics such as collector efficiency and saturated output power capability cannot be obtained using S-parameters [9]. The load line can only be related to the transistor's output impedance in terms of power gain, but it cannot provide any information regarding collector efficiency or saturated output power.

1.1.2 Harmonic Balance Technique

Another popular technique used in simulating non-linear microwave circuits is harmonic balance [5,10]. This approach is limited to steady-state analysis and differs from the time domain methods in that it assumes the response consists of a linear combination of sinusoids.

In the harmonic balance method, the circuit is partitioned into linear and non-linear subnetworks. The linear subnetwork is described in the frequency domain, and the non-linear subnetwork in the time domain as a set of differential equations. In the steady-state, the state variables used to describe the non-linear network are approximated by the sum of harmonically related sinusoids. The coefficients of these sinusoids completely specify the circuit's steady-state operation. The solution is obtained by transforming time domain voltages and currents into the frequency domain using the fast Fourier

transform. These quantities are used to calculate the frequency response of the linear network. A numerical method is used to obtain time domain quantities which have spectral components that satisfy the linear network equations. Hence, the steady-state response is obtained directly, and calculation of the transient response is avoided. Harmonic balance is useful for mildly non-linear circuits driven by sinusoidal sources. For highly non-linear circuits, several sinusoids are necessary to construct an accurate solution, and the efficiency of the method is reduced [10]. This technique may be used to find the steady-state response of an RF PA, but it cannot provide transient analysis for applications such as the digital cellular radio transmitter.

1.1.3 Time Domain Technique

Non-linear circuit simulation in the time domain has been covered extensively in the literature [5]. This work has led to the development of several time domain analysis programs such as SCEPTRE, NET1, BIAS-3, CANCER, SLIC, and SPICE [11]. While these programs were not developed for RF and microwave circuits, programs such as EEsof's mwSPICE™ have emerged with enhanced device models and improved convergence algorithms to accommodate these applications.

In the time domain method, both linear and non-linear portions of the circuit are solved in the time domain. The entire circuit is described in terms of a state vector of voltages and currents, such as a Sparce Tableau matrix. This state vector contains a set of differential equations which is obtained by combining component voltage-current relations with Kirchoff's laws. These equations are solved directly in the time domain using a numerical integration technique. Time domain methods provide the most natural solution to the simulation problem as the actual circuit operates in the time domain [5]. In

addition, semiconductor device operation is most naturally described in the time domain (for example, the continuity and diffusion equations).

There are two main disadvantages of time domain analysis for RF and microwave applications [5]. First, accurate measurement of linear RF components must be carried out in the frequency domain using sinusoidal excitation. These results are usually used to determine parameters for a frequency domain model. Problems arise when an accurate frequency domain model must be converted for use in the time domain. For example [5], a transmission line is best described by frequency-dependent parameters such as the propagation constant (γ) and characteristic impedance (Z_o). In theory, it is possible to convert these models analytically for use in the time domain, but as yet, practical techniques are not available. Therefore, at present, time domain models which are approximations to accurate frequency domain models are used. The other disadvantage of time domain methods is that the numerical techniques used to solve the set of differential equations are relatively inefficient. This is primarily a result of time constants in the circuit which necessitate small time steps in the numerical integration process. In addition, most RF applications have only been concerned with the steady-state operation of the circuit. In a typical simulation, the majority of the time is spent waiting to reach steady-state while the various transients subside. "Shooting methods" have been developed to enhance the performance of time domain simulators by partially avoiding calculation of the transient response. This is accomplished using an algorithm such as the Aprille and Trick steady-state search algorithm [12] to calculate initial conditions from which the network starts in a periodic steady-state. While these methods significantly improve numerical efficiency, the analysis is limited to periodic signals.

In spite of the apparent problems with time domain analysis, this method offers several features which justify its use in this research project. As discussed earlier, semiconductor models are best described in the time domain. An accurate model is required for this project so that thermal effects may be incorporated and distinguished from other dominant effects. As well, time domain analysis is not limited only to sinusoidal excitation or steady-state analysis. This is particularly important for applications such as the digital cellular radio transmitter, where it is desired to observe transient behavior. While transient analysis may not be the most efficient simulation technique, the emergence of powerful engineering workstations is reducing the significance of this factor.

1.2 Fundamental Approaches to RF Transistor Modeling

The success of simulation as a design tool for RF PAs is largely dependent on the accuracy of the transistor models. The choice of a transistor model normally involves a compromise between accuracy and mathematical complexity. Several models of varying sophistication and complexity have been developed for bipolar transistors [13]. The remainder of this section provides an introduction to the three basic approaches which are normally used for these models.

1.2.1 Two-port Models

Two port models represent the transistor as a linear device with one input and one output port [13]. These models do not consider device physics, but characterize the transistor by a parameter set determined from terminal measurements. An example of a two-port model is a small or large-signal

S-parameter characterization of a transistor. This approach is best suited to small-signal applications where non-linear effects may be neglected.

1.2.2 Device Physics Models

The device physics approach uses a set of non-linear partial differential equations to describe transistor operation. These relationships (e.g. Poisson's equation, the diffusion equation, and the continuity equation) are based on solid state physics and provide the most general model of the transistor. The model parameters are physical quantities such as carrier concentrations, doping levels, device geometry, and bias voltages. Boundary conditions at the device terminals are applied to obtain solutions for the equations, and terminal currents may be calculated from the physical quantities.

This approach provides the most general model of the transistor since it includes all linear and non-linear effects. It has limited use, however, since the model parameters cannot be determined from terminal measurements and are not usually given in manufacturer's data sheets. As well, these models are numerically inefficient when the non-linear equations are evaluated in more than one dimension (to obtain improved accuracy).

1.2.3 Equivalent Circuit Models

In the equivalent circuit approach, the transistor is represented as a network of lumped and/or distributed circuit elements. These components approximate various physical relationships within the transistor, as in the device physics model. The network may be linear or non-linear, depending on the application and the required accuracy.

The equivalent circuit representation provides a good compromise between the two port and device physics models. Additional network elements

may be included to obtain the required degree of accuracy. Model parameters are determined from terminal measurements on the actual devices, rather than using typical values given in data sheets. In addition to describing the intrinsic transistor, the equivalent circuit may be extended to include parasitic effects. This is particularly important for RF and microwave devices, where parasitics often assume a major role in the operation of the packaged device [14].

An example of an equivalent circuit model is the bipolar transistor model developed by Ebers and Moll [1,15]. The hybrid-π model is obtained by rearranging the original Ebers-Moll (E-M) model (see Figure 1.1). In this form, it is apparent that the model is based on the physics of the device. Ideal diodes provide the exponential relationship between junction voltages and currents, and the current source describes the transistor action which takes place due to the narrow base region. This DC model may be used to model AC operation by adding network elements to describe charge storage in the transistor [1,16]. The AC E-M model includes elements to represent series resistances, junction capacitances, and diffusion capacitances.

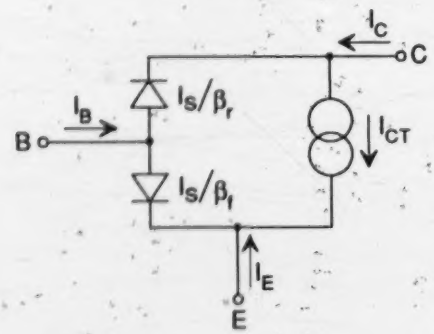


Figure 1.1 Hybrid-π Model

Another equivalent circuit model is based on the charge-control relationship developed by Gummel and Poon [15]. The AC E-M equivalent

circuit model forms the basis for the Gummel-Poon (G-P) circuit model. Second-order effects due to basewidth modulation, high-level injection, and the dependence of the forward transit time on the collector current are incorporated into the G-P model by redefining existing E-M model parameters. These effects are modeled in a unified manner, which produces superior results compared to models which treat them independently. The convenience of the equivalent circuit approach and the enhanced accuracy of the G-P model make it the model of choice for this project.

1.3 Overall Modeling Approach

After the time domain simulation technique using the G-P transistor model was selected, an overall procedure was developed to model the RF transistor and the class B amplifier. This procedure is outlined as follows:

1. Determine DC and AC parameters from DC and low-frequency, small-signal measurements.
2. Estimate forward transit time from small-signal S-parameter measurements taken at several bias points.
3. Measure the thermal dependence of various G-P model parameters.
4. Estimate package parasitics from small-signal RF S-parameter measurements using an assumed network topology and optimization techniques.
5. Determine trimmer capacitor values in the tuned matching networks using small-signal impedance measurements (obtained with a network analyzer) and optimization techniques.

6. Enter the circuit and model parameters into PSpice™, and manually fine-tune the parasitic elements to obtain the best fit to the measured data.
7. Measure junction temperature and incorporate into the simulation, then compare with the measured data.
8. If necessary, fine-tune the transistor model parameters to obtain improved correlation between simulated and measured results.

1.4 Thesis Organization

As indicated above, simulation is an increasingly important tool for the design of RF power amplifiers. The role of simulation will depend primarily on the accuracy and efficiency of active device models. This thesis describes an equivalent circuit approach for modeling an RF power transistor operating as a single-ended class B power amplifier. Specifically, the thermal sensitivity of the G-P model is investigated by including junction temperature as a model parameter in the RF amplifier simulations, and comparing the results to those obtained from an experimental system.

Chapter 2 provides a brief introduction to the semiconductor physics which govern the operation of bipolar junction transistors. Theoretical relationships are derived for a one-dimensional representation, and various assumptions made during the derivations are discussed. The Gummel-Poon charge control relation and the equivalent circuit model are presented. Finally, the simplified version of the G-P model is presented for use in modeling the RF power transistor.

Chapter 3 discusses the extraction techniques used in characterizing the RF power transistors. This includes methods for DC and AC parameters, as

well as parasitic model elements. The structure of the device is discussed, and assumptions made during the characterization are identified. Also, optimization is introduced as a tool for determining model parameters.

The experimental class B amplifier circuit which is used to verify simulation results is introduced in Chapter 4. In addition to discussing the operation of the circuit, various methods of accurately simulating it are introduced. The use of optimization techniques applied to microstrip circuits is presented to ensure that the simulation results are effectively independent of the amplifier circuit models (i.e., any discrepancies between the simulated and measured results may be attributed to transistor model inaccuracies).

Junction temperature measurement techniques are introduced in Chapter 5. Electrical methods are discussed which are able to meet the measurement requirements for the simulation project. A circuit which was developed to measure average junction temperature changes due to internal RF power dissipation is introduced.

Chapter 6 provides a detailed description of the simulation procedure used for the transistor and power amplifier circuit. Results are presented for various operating conditions, in order to compare simulated and experimental operation. The summary of results and conclusions of the thesis are given in Chapter 7. In addition, possible applications of the results are discussed.

2. BIPOLAR JUNCTION TRANSISTOR THEORY AND THE GUMMEL-POON MODEL

This chapter provides an introduction to the operation and modeling of bipolar junction transistors (BJTs). A review of the basic semiconductor physics governing the operation of a BJT is given. This is followed by an introduction to the G-P model. A simplified derivation of Gummel and Poon's charge control relation [15] is presented, including the necessary steps to permit its representation by measurable device parameters.

2.1 BJT Operating Principles

The principle of operation of a bipolar junction transistor is well understood. Numerous sources contain detailed, quantitative descriptions of the semiconductor physics governing the operation of the BJT [1,17]. This section provides a brief summary of these physical relationships.

The BJT is a three-terminal device consisting of two layers of n-type silicon (collector and emitter) separated by a narrow layer of p-type silicon (base), as shown in Figure 2.1 (only the npn BJT is considered here). The transistor can operate in one of four operating regions depending on the polarities of the bias voltages applied to the two pn junctions. The transistor encounters the cutoff, forward active, and saturation regions of operation in the class B amplifier.

In the forward active region, the base-emitter junction is forward biased and the base-collector junction reverse biased. Figure 2.2 shows typical carrier concentrations for the forward active operation along a cross-section of the transistor. The forward-biased base-emitter junction causes free electrons to

be injected into the base region and holes into the emitter region. The emitter is heavily doped compared to the base, and therefore, the current due to injected electrons is much greater than that due to injected holes.

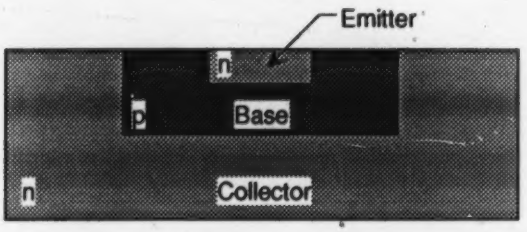


Figure 2.1 NPN BJT (planar structure)

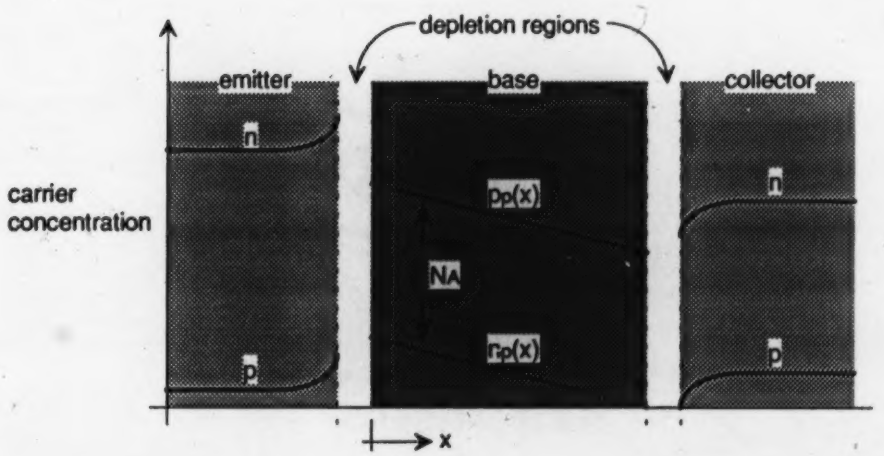


Figure 2.2 Typical Carrier Concentrations for BJT in Forward Active Region (along a cross section of the transistor)

The injected electrons are minority carriers in the base and the excess minority carrier concentration is a maximum at the emitter edge of this region. At the collector edge, this concentration is zero since the reverse-biased base-collector junction causes the electrons to be swept across the depletion region and into the collector. Electrons diffuse from the emitter edge of the

base (high electron concentration) towards the collector. The variation of the excess minority concentration in the base is approximately linear, since the base is usually very thin. This electron diffusion process makes up the primary component of the collector current, I_C, in the transistor under forward bias conditions. Therefore, I_C is proportional to the concentration gradient of the electrons in the base region ($I_C = k \frac{dn_p(x)}{dx}$).

The Boltzmann approximation to the Fermi-Dirac probability function relates the minority carrier concentration at the edge of the base-emitter depletion region to the base-emitter bias voltage. Using the approximation that the concentration of electrons in the base varies linearly from the emitter to collector edges of the base, I_C may be expressed as:

$$I_C = k \bullet \frac{(n_p(0) - 0)}{W_B} = q\,A\,D_n \bullet \frac{\frac{n_i^2}{N_A} e^{(qV_{BE}/kT)}}{W_B} = I_S\, e^{(qV_{BE}/kT)} \qquad (2.1)$$

$$\text{where} \quad I_S = \frac{q\,A\,D_n\,n_i^2}{N_A\,W_B} \qquad (2.2)$$

q = electronic charge
A = cross-sectional area of the emitter
D_n = diffusion constant for electrons (assumed constant)
n_i^2 = intrinsic carrier concentration
N_A = base doping concentration
W_B = base width

The transistor's saturation current, I_S, is often considered to be a constant of the device. However, (2.2) indicates that it is actually a function of the basewidth and the majority carrier concentration in the base.

The current in the base lead consists of two main components. The dominant component is a result of holes which are injected into the emitter from

the base in the same way that electrons are injected from the emitter into the base due to the forward biased base-emitter junction. The other component is a result of recombination in the base, and is proportional to the majority carrier concentration and basewidth. Therefore, the above relationship developed for collector current is applicable for the base current, except that the effective saturation current is much reduced due to the relative doping concentrations. This effective base saturation current is related to the saturation current, I_S, by the transistor's current gain factor, β ($I_{S(base)} = \frac{I_S}{\beta}$). The emitter current is equal to the sum of the base and collector currents.

In the cutoff region, the base-emitter junction is insufficiently biased to produce a significant injection of electrons into the base region. Hence, a negligible collector current is induced, and the transistor operates as an open circuit.

In the saturation region, both pn junctions are forward biased and the operation can be described by the superposition of carrier distributions for the forward and reverse active modes of operation.

2.2 The Gummel-Poon Model

2.2.1 Evolution of the Gummel-Poon Model

The G-P model was introduced in 1970 and is an improved version of the bipolar junction transistor model developed by Ebers and Moll [1,15]. The Hybrid-π model is obtained by rearranging the original Ebers-Moll model (see Figure 2.3). Ideal diodes provide the exponential relationship between the junction currents and voltages, and the current source describes the transistor action which takes place due to the narrow base.

This DC model can be expanded to include AC operation by adding parameters to describe charge storage in the transistor [1,16]. As well, improved DC representation is made possible by including non-ideal components. This augmented model is illustrated in Figure 2.4; non-ideal diodes, series resistances, depletion capacitances, and diffusion capacitances have been added to the basic model. Non-ideal current components are represented by the non-ideal diodes. The resistors model series resistances between the device contacts and the active regions. Depletion capacitors represent the capacitances which result from fixed charges in the depletion regions of the emitter-base and collector-base junctions. Diffusion capacitors model charge storage due to mobile carriers in the transistor which occur under normal bias conditions (see Figure 2.2).

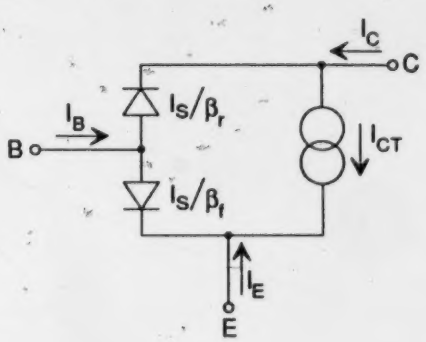


Figure 2.3 Hybrid-π Model

The AC Ebers-Moll model forms the basis for the G-P model. Second-order effects due to basewidth modulation, high-level injection, and the dependence of forward transit time on collector current are incorporated into the model by redefining existing model parameters. These effects are modeled in a unified manner, which produces superior results as compared to models which treat them independently.

Package parasitics are also very important in the operation of transistors at RF and microwave frequencies. To account for these effects, the intrinsic transistor is surrounded by an equivalent parasitic network consisting of reactive elements.

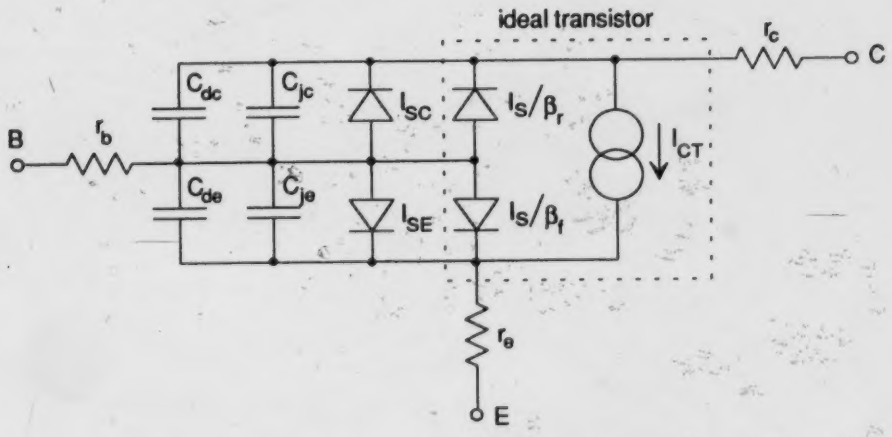


Figure 2.4 AC Ebers-Moll and Gummel-Poon Model Topology

2.2.2 Derivation of the Charge Control Relation

In Section 2.1, an analytical expression was given for the transistor saturation current. This section provides a brief introduction to the charge control relation developed by Gummel and Poon, and derives the expression for I_S which enables basewidth modulation and high-level injection to be included in the model.

The general DC expressions for electron current density, J_n, and hole current density, J_p, in a npn BJT are:

$$J_n = q\,\mu_n\,n(x)\,E(x) + q\,D_n\,\frac{dn(x)}{dx} \qquad (2.3a)$$

$$J_p = q\,\mu_p\,p(x)\,E(x) - q\,D_p\,\frac{dp(x)}{dx} \qquad (2.3b)$$

where μ_n = electron mobility (assumed constant)
μ_p = hole mobility (assumed constant)
$E(x)$ = electric field
D_n = diffusion constant for electrons (assumed constant)
D_p = diffusion constant for holes (assumed constant)
$n(x)$ = free electron concentration
$p(x)$ = hole concentration

These equations make no assumptions regarding the variations of the carrier concentrations, so the results of the derivation are valid for any doping profile. An expression for the electric field is obtained from equation (2.3b) by assuming that the hole current is zero. This is justified since the transistor's doping levels are normally selected so that a forward biased base-emitter junction causes an injection of electrons into the base which is much greater than the injection of holes into the emitter. As well, in the forward active region, the base-collector junction is reverse biased so that no significant hole current crosses it. For other operating regions, the zero J_p assumption is not entirely valid, but the results obtained are usually satisfactory since the value of J_p would be multiplied by a small fraction if retained [1] (except for the high-level injection case [1]). Using the above assumptions and applying the Einstein relationship, the following expression is obtained:

$$p(x)\, J_n = q\, D_n\, n(x) \frac{dp(x)}{dx} + q\, D_n\, p(x) \frac{dn(x)}{dx} \qquad (2.4)$$

Equation (2.4) is simplified using the product rule:

$$p(x)\, J_n = q\, D_n \frac{d}{dx} [n(x)\, p(x)] \qquad (2.5)$$

The electron current density is constant for the DC case since non-ideal diodes are used to represent losses due to recombination. Therefore, it can be determined by integrating both sides of (2.5), with the limits of integration being the base sides of the two depletion regions. These limits are justified since $p(x) \approx 0$ in the emitter and collector regions (holes are minority carriers in these regions) and in the depletion regions, assuming that there are no mobile carriers in these regions. This is different from the original derivation by Gummel and Poon, where they integrate over the entire transistor [15]. However, the differences in the final results are not significant, especially since the model parameters are determined experimentally [1]. Therefore, the current density is obtained from (2.5) as:

$$J_n = \frac{q D_n \int_{x_{e'}}^{x_{c'}} \frac{d}{dx}[n(x)\, p(x)]\, dx}{\int_{x_{e'}}^{x_{c'}} p(x)\, dx} \qquad (2.6)$$

Carrying out the integration in the numerator, using the Boltzmann relations, and multiplying by the cross-sectional area, an expression for the total DC minority current, I_n, is obtained:

$$I_n = -\frac{q D_n A n_i^2 \left(e^{(qV_{BE}/kT)} - e^{(qV_{BC}/kT)} \right)}{\int_{x_{e'}}^{x_{c'}} p(x)dx} \qquad (2.7)$$

This current corresponds to the current generator, I_{CT} in the G-P model (actually $-I_{CT}$ using the model current conventions) , and to equation (2.1)

developed in Section 2.1. Comparing the two equations, it is apparent that (2.7) contains an analytical expression for the saturation current I_S. In the previous expression, the denominator is represented by a constant product ($N_A W_B$). The saturation current, however, is not constant but varies with operating conditions since the limits of integration vary with bias levels and hole concentration.

The integral in the denominator in (2.7), when multiplied by q and cross-sectional area A, represents the total majority charge in the base, Q_B. Gummel and Poon redefine I_S by defining a constant zero-bias, majority base charge, Q_{BO}. This represents the value of the integral in (2.7) when zero bias is applied to both pn junctions. The normalized majority base charge, q_b, is defined as the ratio of the majority charge in the base, Q_B, to this zero-bias value. Multiplying (2.7) by Q_{BO}/Q_{BO} and rearranging terms, the expression for collector current may be expressed as:

$$I_{CT} = \frac{q D_n A n_i^2}{\int_{x_{eo'}}^{x_{co'}} N_A \, dx} \cdot \frac{1}{q_b} \left(e^{(qV_{BE}/kT)} - e^{(qV_{BC}/kT)} \right) \qquad (2.8)$$

where $x_{eo'}$ and $x_{co'}$ represent the zero-bias values of x_e and x_c, respectively.

The first term in (2.8) is a fundamental constant of the device, I_{SS}, which is fixed by the transistor's doping profile. Therefore, the expression for I_{CT} can be rewritten as:

$$I_{CT} = \frac{I_{SS}}{q_b} \left(e^{(qV_{BE}/kT)} - e^{(qV_{BC}/kT)} \right) \qquad (2.9)$$

This is the charge control relationship developed by Gummel and Poon. Although it is similar to the expression used in the Ebers-Moll model, the

normalized majority base charge term is a variable which represents second-order effects. This term can be represented by measurable device parameters, as described in the next section.

2.2.3 Representation of q_B by Measurable Model Parameters

The total majority charge in the base, Q_B, can be represented as the sum of a zero-bias component and a second component which depends on the bias levels and high-level injection effects. The operating-point-dependent component can be further divided into four subcomponents; two represent the dependence of Q_B on basewidth changes due to non-zero bias voltages, and two represent variations in Q_B due to high-level injection effects. This is expressed analytically as:

$$Q_B = q A \int_{x_{eo'}}^{x_{co'}} N_A \, dx + q A \left[\int_{x_e(V_{B'E'})}^{x_{eo'}} N_A \, dx + \int_{x_{co'}}^{x_C(V_{B'C'})} N_A \, dx \right]$$

(zero-bias) *(basewidth modulation)*

$$+ q A \left[\int_{x_e(V_{B'E'})}^{x_c(V_{B'C'})} (p_f(x) - N_A) \, dx + \int_{x_e(V_{B'E'})}^{x_c(V_{B'C'})} (p_f(x) - N_A) dx \right] \qquad (2.10)$$

(high-level injection)

$$= Q_{B0} + Q_E + Q_C + Q_F + Q_R \qquad (2.11)$$

Although Q_B can be divided into five components, these do not exist independently (except for Q_{B0}). This can be seen by considering Q_F and Q_E. Q_F represents the excess majority charge in the base region due to high-level injection when a non-zero base-emitter voltage, $V_{B'E'}$, is applied. This same

bias voltage, however, also causes an increase in the excess majority charge in the base (Q_E), since the edge of the base-emitter depletion region is moved from the zero-bias position of $x_{eo'}$ to $x_e(V_{B'E'})$.

Normalized majority base charge, q_b, is required for evaluation of the charge control relation, and is redefined as:

$$q_b = 1 + q_e + q_c + q_f + q_r \tag{2.12}$$

where the lowercase "q" terms correspond to the normalized Q_B terms.

The remainder of this section presents how these charge components may be represented by measurable model parameters.

q_c represents the portion of the majority base charge which results from basewidth modulation by the base-collector voltage. In the forward active region, the base-collector junction is reverse biased, and the depletion region is extended towards the base. Therefore, q_c is negative and may be calculated by considering that the removed base charge (relative to the zero-bias case) is exactly the same as the charge now stored in the depletion region (assuming low current levels). Therefore, q_c can be calculated from the base-collector junction capacitance as:

$$q_c = \frac{1}{Q_{B0}} \int_0^{V_{B'C'}} C_{jC}(V)\, dV \tag{2.13}$$

Assuming $C_{jC}(V)$ is constant, (2.13) is evaluated as:

$$q_c = \frac{C_{jC}}{Q_{B0}} V_{B'C'} = \frac{V_{B'C'}}{V_A} \tag{2.14}$$

V_A is the Early voltage and is defined by expression (2.13) divided by the base-collector bias voltage, $V_{b'c'}$. A similar procedure is used to define the reverse Early voltage, V_B, by considering the q_e component of q_b. Therefore, basewidth modulation is described by two model parameters, the forward and reverse Early voltages. Although the assumption of a constant C_{jC} (C_{jE} for q_e) is not accurate for all bias conditions, a detailed analysis [1] has shown that the errors introduced are small compared to q_b. A more precise model for q_c (or q_e) may be derived by using a more complex model for the junction capacitance in (2.13). This is a strength of the G-P model, since it indicates exactly how a more accurate solution may be obtained (unlike others, such as the Ebers-Moll model where enhancements are not as obvious [1]).

q_f represents the excess majority charge in the base region due to high-level injection when a non-zero base-emitter voltage is applied. This charge corresponds to the carrier distribution which causes the flow of collector current due to diffusion. Therefore, q_f is proportional to the collector current and is expressed as the collector current multiplied by the average base transit time (and normalized with respect to Q_{B0}). Similarly, q_r is expressed as the product of reverse collector current and a reverse average transit time (also normalized with respect to Q_{B0}).

q_b can now be expressed using the above developed relationships as:

$$q_b = 1 + \frac{V_{B'E'}}{V_B} + \frac{V_{B'C'}}{V_A} + \frac{\tau_B I_{SS}}{Q_{B0}} \frac{(e^{(qV_{B'E'}/kT)} - 1)}{q_b} + \frac{\tau_{BR} I_{SS}}{Q_{B0}} \frac{(e^{(qV_{B'C'}/kT)} - 1)}{q_b} \qquad (2.15)$$

A test for the high-level injection condition may be derived if the first three terms of (2.15) are defined as q_1, and the last two terms as q_2/q_b. The expression for q_b can then be rewritten as [1]:

$$q_b = q_1 + \frac{q_2}{q_b} \tag{2.16}$$

and

$$q_b = \frac{q_1}{2} + \sqrt{\left[\frac{q_1}{2}\right]^2 + q_2} \tag{2.17}$$

When $q_2 << \frac{q_1^2}{4}$, $q_b \approx q_1$, corresponding to the low-level injection condition. High-level injection occurs when $q_2 >> \frac{q_1^2}{4}$, and hence, $q_b \approx \sqrt{q_2}$.

The evaluation of the high-level injection components to arrive at model parameters proceeds by inserting the $q_b \approx \sqrt{q_2}$ approximation into the charge control relation (2.9). The result is:

$$I_{CT} = \sqrt{\frac{Q_{B0}\, I_{SS}}{\tau_B}}\; e^{(qV_{BE}/2kT)} \tag{2.18}$$

Equation (2.18) indicates that the collector current is proportional to $e^{(qV_{BE}/2kT)}$ in the high-level injection region. Therefore, collector current behavior is known at the low and high-level injection regions. In the transition from low to high-level injection, the behavior deviates from the two asymptotic relationships. The knee current, I_K, and the knee voltage, V_K, are defined as the point of intersection between the low and high-level injection asymptotes. Solving for this point:

$$I_K = \frac{Q_{B0}}{\tau_B} \tag{2.19}$$

A similar analysis can be performed for the inverse operating region, and the reverse knee current, I_{KR}, is of the same form as in (2.19).

Finally, q_2 can now be written as:

$$q_2 = \frac{I_{SS}}{I_K} \frac{(e^{(qV_{B'E'}/kT)} - 1)}{q_b} + \frac{I_{SS}}{I_{KR}} \frac{(e^{(qV_{B'C'}/kT)} - 1)}{q_b} \qquad (2.20)$$

The normalized majority base charge, q_b, is now represented by five measurable model parameters (I_{SS}, V_A, V_B, I_K, I_{KR}). These are all determined from a series of DC measurements. The remainder of the G-P parameters correspond to those of the modified AC Ebers-Moll model. Characterization of the RF power transistor using the G-P model is discussed in the next chapter.

3. CHARACTERIZATION OF RF POWER TRANSISTORS

The accuracy of a transistor model is largely dependent on the accuracy of the model parameters. This chapter outlines a method for extracting the G-P model parameters, and for characterizing the package parasitics. A series of DC and small-signal measurements are combined with computer-aided analysis and optimization techniques to determine optimal model parameter values. Several parameters are measured versus temperature, and the results are compared with previously developed temperature relationships [18]. Special measurement techniques and the difficulties associated with them are described.

Experimental results obtained for an RF power transistor are presented, and the significance of the device's internal structure is discussed. Two main error sources in the extraction of the model parameters are discussed; errors which result from approximations made while deriving the extraction techniques, and errors which result from inaccuracies in the physical measurement systems.

The significance of parasitic effects on the operation of an RF BJT is discussed, with particular emphasis placed on the use of optimization to deduce the critical component values from measured S-parameters.

3.1 Transistor Description

The Philips BLV93 RF power transistor was used in the experimental class B power amplifier. This npn planar device is designed for common emitter operation at the 800 to 1000 MHz frequency range. The device consists of eight transistors connected in parallel as shown in Figure 3.1. An

interdigitated design is used for the individual transistors (40 emitter fingers). The emitter fingers are processed to have a higher resistivity than the normal emitter region. This structure, as shown in Figure 3.2, is functionally equivalent to a transistor with multiple emitters and ballast resistors. These ensure an even distribution of current throughout the device [19]. and hence, a uniform temperature profile. Although emitter resistance decreases the transistor's gain, the large number of emitter sites on the composite device reduce this effect.

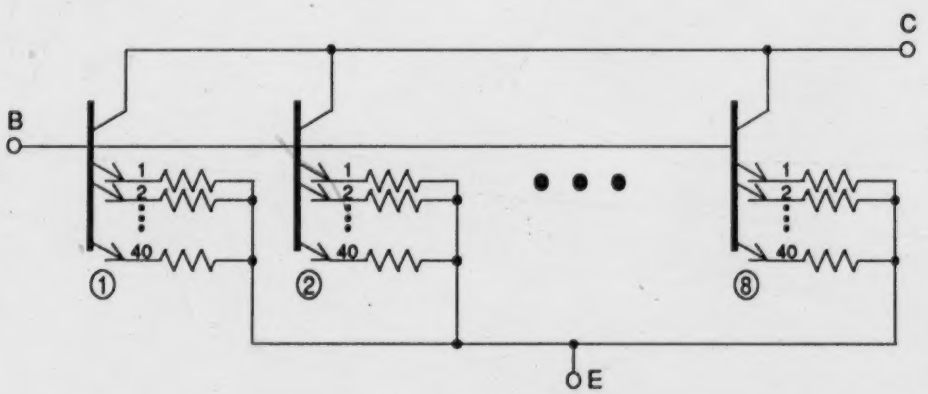


Figure 3.1 Internal Structure of the BLV93 RF Power Transistor

The eight transistors are contained on two separate chips (four transistors per chip). While the transistors on a given chip can be assumed to be matched, this may not be the case for those on different chips. Thus, the most accurate BLV93 model should include two large-area transistors with passive networks to describe the inter-transistor and package parasitics. This complex model was not implemented, however, as is was not possible to make measurements on the individual chips. In addition, it is desirable to use a relatively simple model in order to minimize the number of parameters, and to provide a model which is computationally efficient. Hence, the transistor is

represented as a single, large-area device which is embedded in a discrete parasitic network.

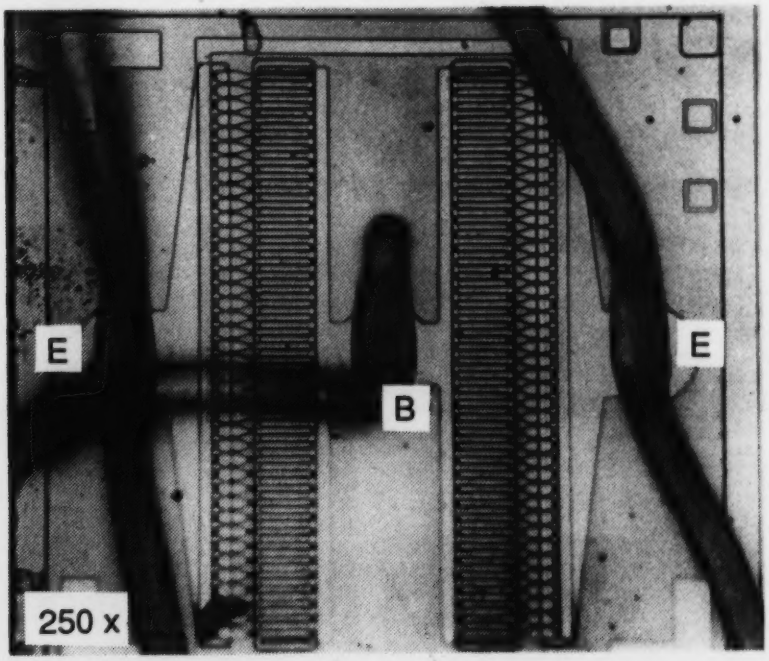


Figure 3.2 BLV93 Individual Transistor Layout

The transistor chips are mounted in a SOT-171 flange-mounted package. This package provides good heatsinking capabilities, and uses microstrip leads to reduce discontinuities when connecting to the amplifier circuit. Four emitter leads provide a low-inductance emitter connection, which is particularly important for RF and microwave devices to provide maximum gain and ensure stability.

3.2 Parameter Extraction Techniques

In Chapter 2, the G-P model was shown to provide DC and AC parameters which describe device operation based on semiconductor physics.

The implementation of this model in PSpice includes a total of 55 parameters. There are 18 DC parameters and 14 AC parameters which correspond directly to the G-P model. Most of the additional parameters are used in empirical relationships which have been added to compensate for the distributed nature of various model parameters, and for temperature effects.

The relatively large number of DC parameters is a result of the general form of the model provided by PSpice; virtually all parameters in the analytical current expressions are provided as variables. For example, the forward emission coefficient, η_F, is assumed to be equal to 1, and is normally not shown in the expressions. However, PSpice includes this as a model parameter which can be specified by the user.

The large number of AC parameters is also a result of the general form of the model. Empirical relationships are included to describe the dependence of forward transit time on bias voltages, collector current, etc. Only the AC parameters which correspond directly to the G-P model were measured and included in the simulation.

3.2.1 DC Parameters

Techniques have been developed for extracting parameter values from DC terminal measurements [1,20]. DC parameters were determined using these procedures and variations of them.

The standard DC G-P model parameters and their typical values for the BLV93 are shown in Table 3.1. Several of these are determined directly from forward and reverse Gummel plots ($\log(I_C)$ and $\log(I_B)$ versus V_{BE}). Since the DC voltage-current relationships are exponential, they appear as straight lines on the Gummel plots. The boundaries between the various operating regions

and the effects of various non-ideal model components are indicated by deviations from these straight lines.

Symbol	Parameter Name	BLV93 Value
I_{SS}	saturation current	1.20×10^{-14}
I_{SE}	base-emitter leakage saturation current	2.56×10^{-13}
I_{SC}	base-collector leakage saturation current	6.34×10^{-14}
η_F	forward emission current coefficient	1
η_R	reverse emission current coefficient	1
η_{EL}	base-emitter leakage emission coefficient	1.40
η_{CL}	base-collector leakage emission coefficient	1.12
β_F	ideal maximum forward current gain	75
β_R	ideal maximum reverse current gain	7
V_A	forward Early voltage	78 V
V_B	reverse Early voltage	∞
I_K	forward knee current	∞
I_{KR}	reverse knee current	∞
r_c	collector resistance	0.67 Ω
r_e	emitter resistance	0.13 Ω
r_b	base resistance	1.50 Ω

Table 3.1 Standard DC Gummel-Poon Model Parameters in PSpice

In determining model parameters, it is important to ensure that all second-order effects are minimized and may therefore be neglected (as assumed in the derivation of the extraction techniques). For example, when characterizing ideal diode behavior, the correct region on the Gummel plot must be used so that non-ideal diode, basewidth modulation, high-level injection, and resistive effects are minimized.

3.2.1.1 *Diode Characteristics*

In order to avoid basewidth modulation effects in the characterization of the forward ideal and non-ideal diodes, a circuit was designed to hold $V_{BC} \approx 0$ (see Figure 3.3). This feedback circuit keeps the base to ground and collector to ground voltages equal, and the high input impedance amplifier (TL074) ensures that errors introduced in the current measurements are negligible. This configuration is also desirable since the low collector voltage minimizes self-heating effects, even when measuring collector currents in the 1A range. The reverse operating region is measured by interchanging the collector and emitter connections.

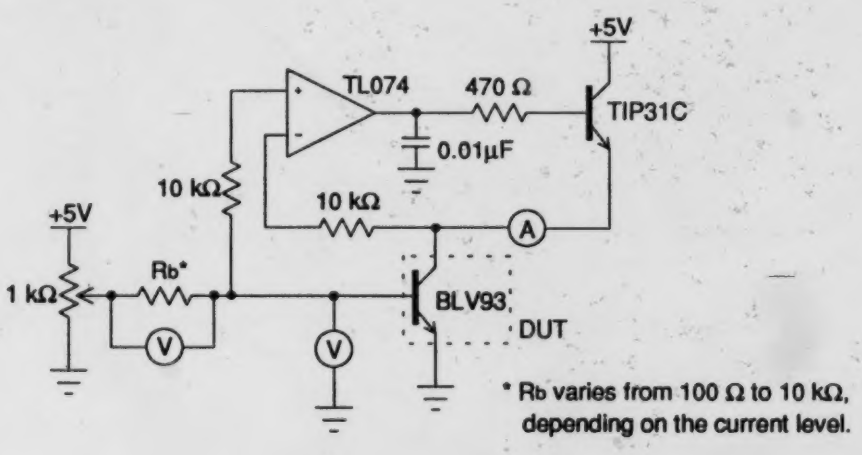


Figure 3.3 Circuit for DC Diode Operation Measurements

I_{SS} is determined by extrapolating the collector current in the forward Gummel plot to $V_{BE} = 0$ [20]. This operation is performed numerically to avoid inconsistencies which result from applying a graphical technique to a logarithmic plot. The forward emission coefficient is also derived numerically from the forward Gummel plot.

The maximum ideal forward current gain, β_F, is obtained from base and collector current measurements in the forward active region. The maximum value is used as the model parameter, and deviations from this value are represented by non-ideal low and high current effects. The maximum ideal reverse current gain, β_R, is obtained from reverse current measurements.

The forward non-ideal diode characteristics are described by I_{SE} and η_{EL}. In the low current region, base current is expressed as:

$$I_B \approx \frac{I_{SS}}{\beta_F} e^{(qV_{BE}/kT)} + I_{SE} e^{(qV_{BE}/\eta_{EL}kT)} \qquad (3.1)$$

The non-ideal diode parameters are usually determined graphically by neglecting the first term in equation (3.1) and extrapolating the base current value at $V_{BE} = 0$ [20]. η_{EL} is the obtained from the slope of the curve in the low current region. This method was found to be inaccurate for the BLV93 since the ideal base current component is not negligible in the low-current region.

Instead, a numerical technique was used to include the full base current expression of (3.1). Using the extracted values for I_{SS} and β_F, and assumed values of η_{EL} ranging from 1 to 1.5, I_{SE} is calculated from (3.1) for three measured data points (I_B, V_{BE} pairs). The optimal value of η_{EL} is obtained when the calculated values of I_{SE} are equal for each of the three data points (this also specifies the optimal value of I_{SE}). The results of this method are much superior to those of the graphical technique.

Measured reverse active region data are used in conjunction with the above numerical technique to determine the corresponding reverse non-ideal diode parameter values. A typical Gummel plot for the forward active region is shown in Figure 3.4. Deviations at the high current region are a result of bulk resistances and second-order effects.

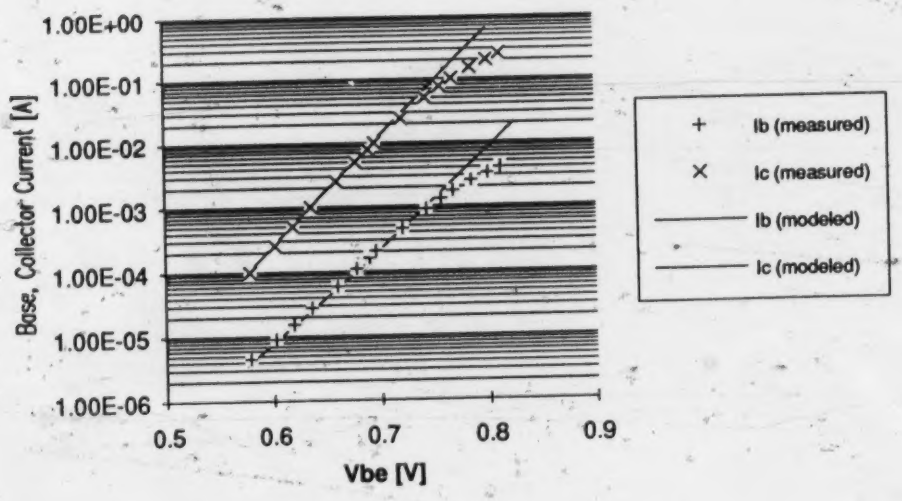


Figure 3.4 Typical Gummel Plot (simple diode model)

3.2.1.2 *Basewidth Modulation and High-Level Injection Parameters*

The forward Early voltage is determined from a plot of I_C versus V_{CE} [20]. A numerical technique was implemented to calculate the Early voltage at several operating points; the average value was used as the model parameter. The reverse Early voltage was not modeled as it is not critical for the simulation of the class B amplifier.

The forward knee current is equal to the value of I_C where the forward current gain falls to half of its maximum value in the high-current region [20]. This point was not observed in the measured data, and hence, high-level injection effects were neglected. This observation is also supported by information in the BLV93 data sheet, which indicates an I_K of approximately 5 A (see Appendix A). Similarly, the reverse knee current was not included in the model.

3.2.1.3 *Bulk Resistances*

One of the most difficult groups of parameters to determine is the bulk resistances. This is primarily due to the fact that these elements provide only a rough approximation to the actual physical processes which they represent. As well, various sources [1,18] emphasize the importance of using a measurement technique in which the transistor operates close to the actual mode of operation. This is difficult for the large-signal RF amplifier case, and therefore only approximate resistance parameters can be determined.

r_c represents the total resistance between the collector terminal and the active collector region. It is difficult to obtain an accurate value for this parameter, since it is dependent on the collector current distribution as determined by the operating point. Two limiting values for r_c are the normal active region value, and the saturation region value. Since the transistor operating as a class B amplifier experiences both of these operating regions, the optimal parameter value should be between these two extremes.

Results of previous work have shown that the voltage drops across the transistor junctions are nearly identical when configured as shown in Figure 3.5 [21]. Since the collector is open circuited and $V_{BE} \approx V_{BC}$, the measured value of V_{EC} is a result of the base current flowing through the collector resistor. This technique provides an estimate of the collector resistance in the active region, and represents an upper limit for r_c.

The emitter resistance, r_e, is represented adequately by a lumped resistor since it is dominated by the metal contact resistance. The procedure used to measure r_c is used for r_e by interchanging the collector and emitter terminals.

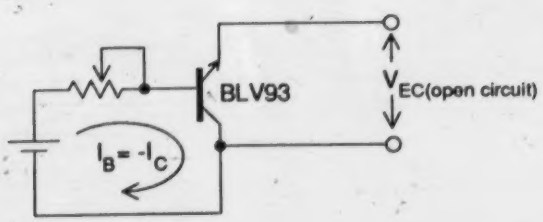


Figure 3.5 r_c Measurement Circuit

r_b represents the resistance between the base terminai and the active base region. This is a difficult parameter to determine since, although it is modeled as a single, lumped element, it is actually a variable resistance consisting of two main components [17]. The extrinsic component is the portion of the base current corresponding to the current path between the base lead and the active base region. This part of r_b is relatively constant and is accurately represented by a fixed resistance. The intrinsic component corresponds to the voltage drop in the active base region which is necessary to drive the majority carrier current. This part of r_b is very non-linear since it results from the integrated effect of the distributed voltage drop in the active base region. The intrinsic base resistance is further complicated by current crowding, which tends to reduce the base resistance value by causing the majority of the base current to flow in the active region close to the base contact.

The value of r_b determined using parameter extraction techniques is a strong function of the technique used [1]. Since there is no available technique which closely approximates RF class B operation, r_b was estimated from DC voltage-current measurements and the previously determined parameter values.

Measured and simulated Gummel plots are shown in Figure 3.6, with all DC parameters included in the model.

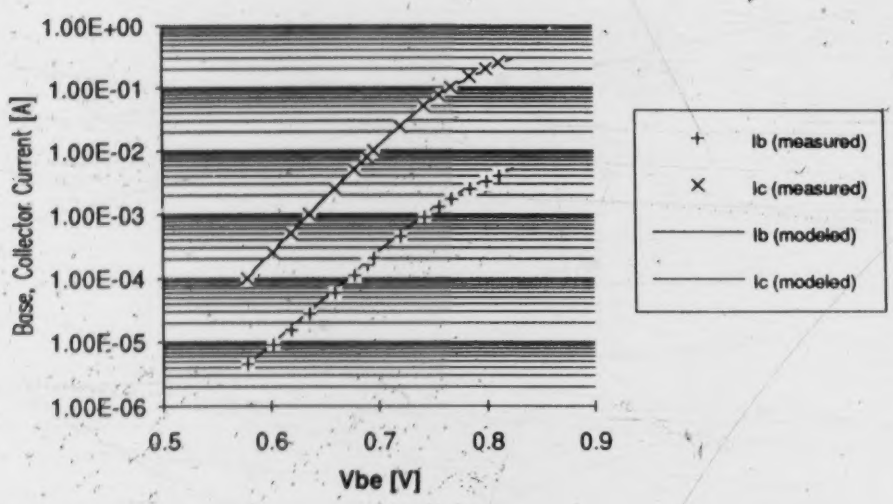


Figure 3.6 Simulated and Measured Gummel Plots (final DC model)

3.2.2 Thermal Characterization of DC Model Parameters

The temperature dependence of several DC G-P model parameters has been described in earlier work [18], and several of these are included in the PSpice implementation of the G-P model. Specifically, temperature relationships are provided for I_{SS}, I_{SE}, I_{SC}, β_F, β_R, r_e, r_b, and r_c.

Measurement techniques presented in the previous section were used to measure I_{SS}, I_{SE}, and β_F versus junction temperature. The circuit configuration ensures that self-heating effects are small ($P_{diss(max)} < 1$ W), so that the junction temperature may be assumed to be equal to the heatsink temperature. The three parameters were measured over a temperature range of 20 °C to 80 °C. The results were observed to agree very well with the PSpice models, as shown in Figures 3.7 and 3.8.

The reverse parameters I_{SC} and β_R were not measured versus temperature as their effects are not significant for the class B amplifier. Since

there is considerable uncertainty in the measured values of the bulk resistors, no attempt was made to determine the corresponding empirical temperature model parameters included in PSpice.

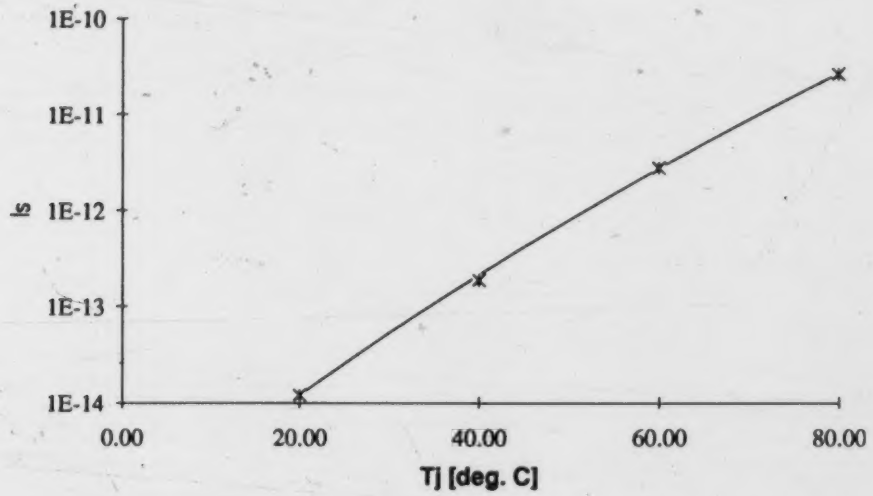


Figure 3.7 Saturation Current versus Junction Temperature

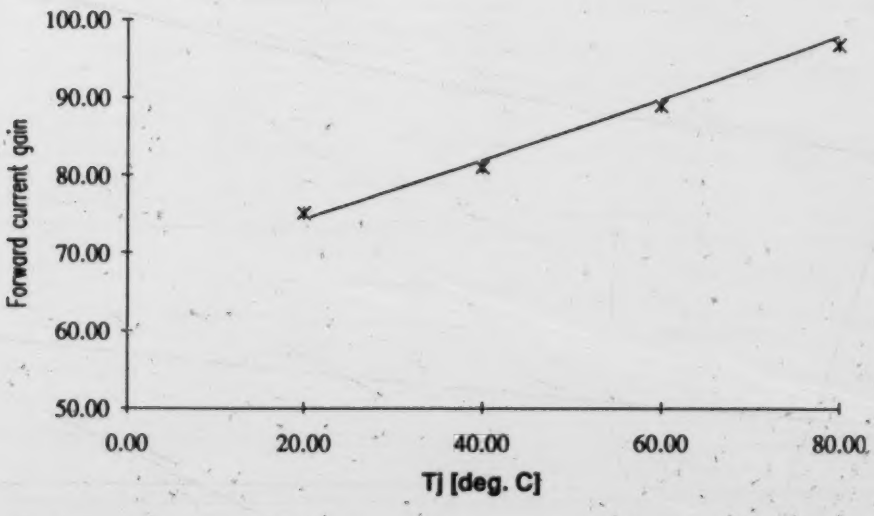


Figure 3.8 Forward Current Gain versus Junction Temperature

3.2.3 AC Parameters

Charge storage is modeled by non-linear junction and diffusion capacitors. The standard AC G-P model parameters and their values for the BLV93 BJT are shown in Table 3.2.

Symbol	Parameter Name	BLV93 Value
C_{je}	zero-bias base-emitter junction capacitance	72.0 pF
ϕ_e	base-emitter junction built-in potential	0.57 V
m_e	base-emitter junction grading coefficient	0.52
C_{jc}	zero-bias base-collector junction capacitance	28.9 pF
ϕ_c	base-collector junction built-in potential	0.47 V
m_c	base-collector junction grading coefficient	0.57
τ_F	ideal forward transit time	50 ps
τ_R	ideal reverse transit time	0

Table 3.2 Standard AC Gummel-Poon Model Parameters in PSpice

3.2.3.1 *Junction Capacitance Measurements*

An HP4192A impedance analyzer was used to measure the junction capacitances as a function of reverse bias voltage. A test fixture was constructed to make the transistor package compatible with the instrument. Parasitic effects introduced by this fixture were nulled using a built-in calibration routine prior to inserting a device for measurement. All measurements were taken at 1 MHz to avoid effects due to ohmic resistances.

The test results indicated relatively large stray capacitances since the junction capacitance approached a non-zero value as the reverse bias was increased. The measured capacitance is of the form:

$$C_{j(measured)} = \frac{C_{j0}}{\left(1 - \frac{V}{\phi}\right)^m} + C_{par} \qquad (3.2)$$

The observed parasitic component, C_{par}, complicates the determination of the three varactor relation parameters. A graphical technique was used to determine a set of parameter values which provided satisfactory correlation between the measured data and the relationship of (3.2). The chosen parameter set is not unique, however, and grading coefficients which are slightly greater than 0.5 were obtained. While the grading coefficients are assumed to be between 0.33 and 0.5, it is sometimes necessary to use values outside of this range to obtain a satisfactory curve fit [1]. Typical simulated and measured base-emitter junction capacitance results are shown in Figure 3.9.

The values of the parasitic capacitances, as determined using the above procedure, were not used explicitly in the model. Separate measurements were used to determine parasitics as outlined in Section 3.2. The values obtained in this step, however, were used to confirm the results obtained by the parasitic characterization process.

3.2.3.2 *Diffusion Capacitance Measurements*

As discussed in Chapter 2, diffusion capacitances are specified by the forward and reverse transit time parameters.

τ_F is determined from the transistor's unity gain bandwidth, f_T. This is the frequency at which the small-signal current gain drops to unity, when driving a short circuit load. Since accurate short circuits are difficult to achieve at RF and microwave frequencies, measurements are normally taken below f_T, and the curve is extrapolated. Once f_T is known, τ_F is estimated from [18]:

$$\tau_F = \frac{1}{2\pi f_T} - C_{jc}\, r_c \qquad (3.3)$$

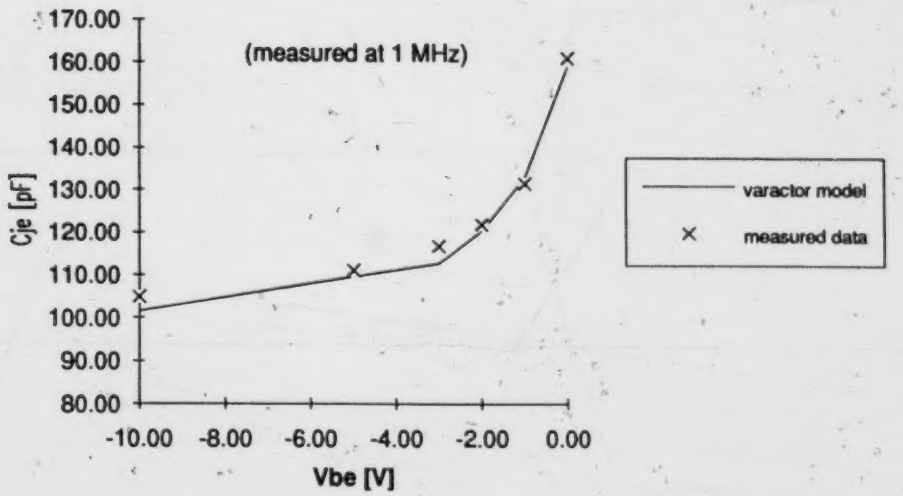


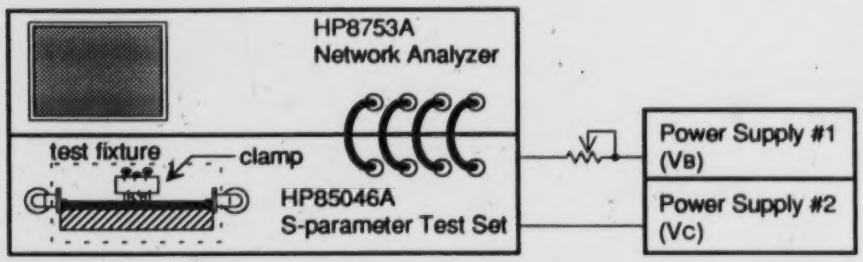
Figure 3.9 Base-emitter Junction Capacitance

f_T was obtained from S-parameter data measured with an HP8753A network analyzer and an HP85046A S-parameter test set. The use of S-parameters is desirable at RF and microwave frequencies, since they do not require open or short circuit terminations. Instead, 50 Ω terminations are used which can be built to be accurate at high frequencies. Also, the transistor is more likely to be stable when driving a 50 Ω load, than when a short circuit load is used.

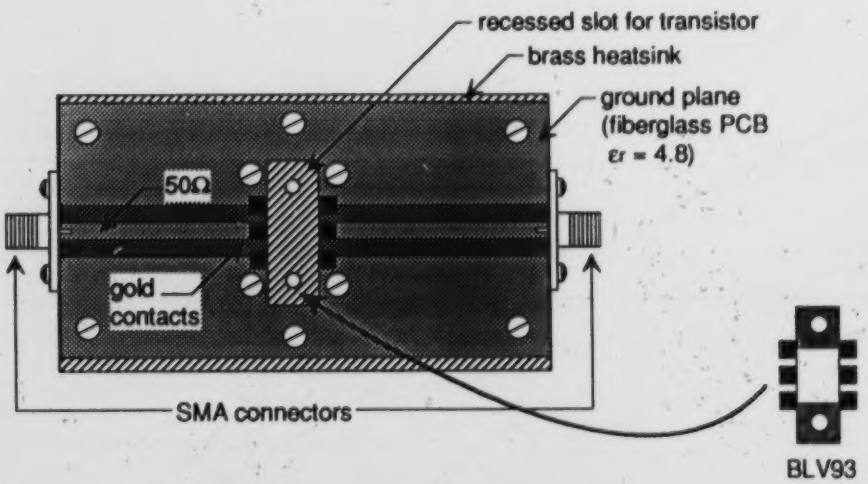
A custom test fixture was designed to connect the transistor to the S-parameter Test Set, as shown in Figure 3.10. Gold contacts are used at the transistor terminal sites to provide low resistance connections without soldering the transistor to the board. An acrylic clamp holds the transistor in place, and provides tight clamping of the transistor leads to the printed circuit board.

Mounting the transistor in the test fixture causes a transformation of the device characteristics through an intermediate network of transmission lines and connectors. De-embedding the transistor parameters is difficult since a large number of calculations is required to translate the reference plane to the device terminals. Also, discontinuities at the connector junctions and non-ideal transmission line behavior are difficult to characterize accurately. The HP8753A network analyzer has sophisticated calibration routines to compensate for these effects. The full two-port calibration routine accounts for discontinuities and non-ideal frequency response in both reflection and transmission measurements. Calibration is achieved by connecting known standard terminations (opens, shorts, and 50 Ω loads) at the desired measurement reference plane, and running internal software routines. This procedure is limited, however, to points in the circuit which are connectorized. Therefore, the network analyzer can be calibrated up to the test fixture connectors with the standard calibration kit, but not to the transistor terminals, as desired.

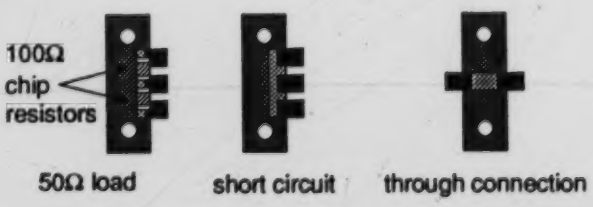
A set of "standard" terminations were made to provide an approximate calibration of the network analyzer to the transistor terminals. Open circuit, short circuit, and 50 Ω (matched) terminations enable calibration of the reflection measurements. A through connection is used to remove losses in the forward and reverse transmission paths. These "standard" terminations were made from pieces of laminated circuit board, which are physically the same size as the transistor package. (The open circuit termination was not constructed, instead it was realized by leaving the 50 Ω transmission lines unterminated. This method provided calibration accuracy which was approximately the same as that achieved when using the calibration kit standard at the network analyzer ports.) The terminations use gold contacts



(a) Test Setup



(b) Test fixture (top view)



(c) Terminations for network analyzer calibration

Figure 3.10 S-parameter Measurement Set-up and Custom Fixture

and are clamped to the test fixture in the same manner as the normal device. While these "standards" are not as precise as those provided with the instrument, the calibration procedure produces very consistent results. The accuracy of the reflection calibration was not determined, but the forward and reverse transmission characteristics were observed to be accurate up to approximately 1.5 GHz (up to this frequency, transmission losses were less than 0.5 dB using the "standard" through connection).

Upon completion of the calibration phase, the device under test is inserted and biased for class A operation (bias ports are provided on the S-parameter test set). Application of small signals ensures that the device operates linearly.

The value of f_T is obtained from the small-signal current gain by assuming a hybrid-π model and a single-pole frequency response for the forward current gain. The small-signal current gain is calculated from the measured S-parameter data using standard conversion formulas. Therefore,

$$\beta_{AC} = h_{21} = \frac{-2\,S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}\,S_{21}} \qquad (3.4)$$

The assumed -20 dB/decade rolloff in β_{AC} was only approximately observed in the measured results, but the estimated value of f_T was consistent with the typical value given in the data sheet (see Appendix A). The deviation from the assumed response is attributed to the simple transistor model, and no attempt was made to develop a more sophisticated model.

Package parasitics also complicate the determination of the f_T for the intrinsic transistor. Thus, the value obtained using this procedure is only an estimate of the actual parameter value. Due to the difficulties in measuring f_T,

further characterization of τ_F as a function of bias voltages and current levels was not attempted.

Since the base-collector diffusion capacitance is proportional to reverse collector current, τ_R was neglected for the purpose of modeling the class B amplifier.

3.2.4 Thermal Characterization of AC Model Parameters

3.2.4.1 *Junction Capacitance*

The G-P model does not provide temperature relationships for the AC parameters. However, since the junction capacitances are modeled using the standard varactor relationship, an expression based on the temperature variation of the barrier potential can be used. Barrier potential and junction capacitance temperature relationships are given as [18]:

$$\phi(T) = \frac{T}{T_{nom}} f(T_{nom}) - 2\frac{kT}{q}\ln\left(\frac{T}{T_{nom}}\right)^{1.5} - \left(\frac{T}{T_{nom}} E_g(T_{nom}) - E_g(T)\right) \quad (3.5)$$

$$C_j(T) = C_j(T_{nom})\left[1 + m_j\left[400 \times 10^{-6}\,(T - T_{nom}) - \frac{\phi(T) - \phi(T_{nom})}{\phi(T_{nom})}\right]\right] \quad (3.6)$$

where T_{nom} = nominal temperature at which parameters were measured.

These relationships were not confirmed by measurements, but were used in the PSpice simulation.

3.2.4.2 *Diffusion Capacitance*

A relationship for the temperature dependence of forward transit time can be derived based on the temperature variation of the basewidth [1].

However, this model is not incorporated in the PSpice BJT model. Therefore, measurements were performed in order to characterize τ_F versus temperature.

As described in Section 3.2.3.2, τ_F is determined from the transistor's unity gain bandwidth, f_T (measured with a network analyzer). Although package parasitics complicate the determination of f_T, they are virtually independent of temperature. Therefore, variations in the measured S-parameters with junction temperature indicate changes in the operating characteristics of the active device.

The small-signal S-parameters were measured versus junction temperature over a range of approximately 4 °C to 47 °C. A CO_2 cooler was built to provide a variable flow of cold air around the transistor and its heatsink. An electrical temperature measuring circuit was used to monitor the junction temperature, and to indicate when the air flow required adjustment (open loop control). Results for S_{11}, S_{21}, and S_{22} are shown in Figures 3.11, 3.12, and 3.13, respectively (the magnitude of S_{12} was very small, and could not be determined accurately by the network analyzer). The increase in S_{21} with frequency corresponds to the decrease in S_{11} with frequency, which is a result of the BLV93's built-in matching network.

The measurements indicate that the small-signal S-parameters are only weak functions of temperature. However, this does not necessarily imply that f_T (and hence τ_F) is also a weak function of temperature. Since the magnitudes of the transistor's input and output reflection coefficients are relatively high (0.6 to 0.8, with respect to the 50 Ω system), a significant amount of the input power is reflected back to the network analyzer. Therefore, changes in the active device characteristics which occur due to variations in junction temperature are masked by the large mismatch at the device terminals (i.e. the parasitic network). In addition, the active device characteristics are transformed by the

parasitic network. This transformation can desensitize the response at the device terminals to changes in the active device.

The variation of S_{11} with junction temperature was less than 2% in magnitude, and less than 2 ° in phase. These changes are of the same order as the measurement accuracy provided by the network analyzer, and therefore, provide little information about the temperature dependence of S_{11}. A similar variation was observed in S_{22} over the measured temperature range.

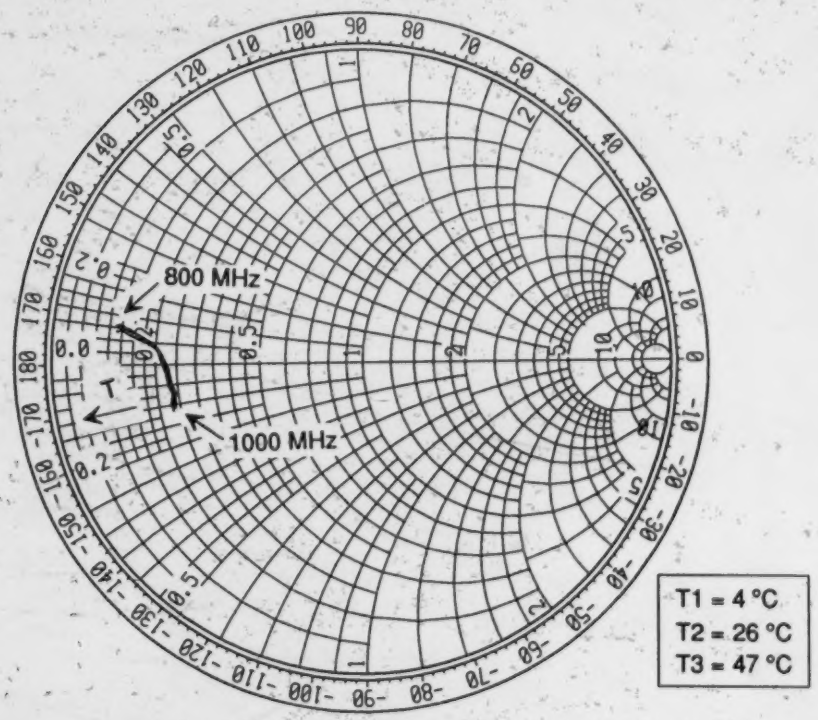


Figure 3.11 S_{11} versus Junction Temperature

Variations in the forward gain of the active device (S_{21}) with temperature are not significantly affected by the mismatch at the device terminals. The BLV93's internal input matching network is primarily responsible for the observed S_{21} frequency response, however, it does not affect the gain

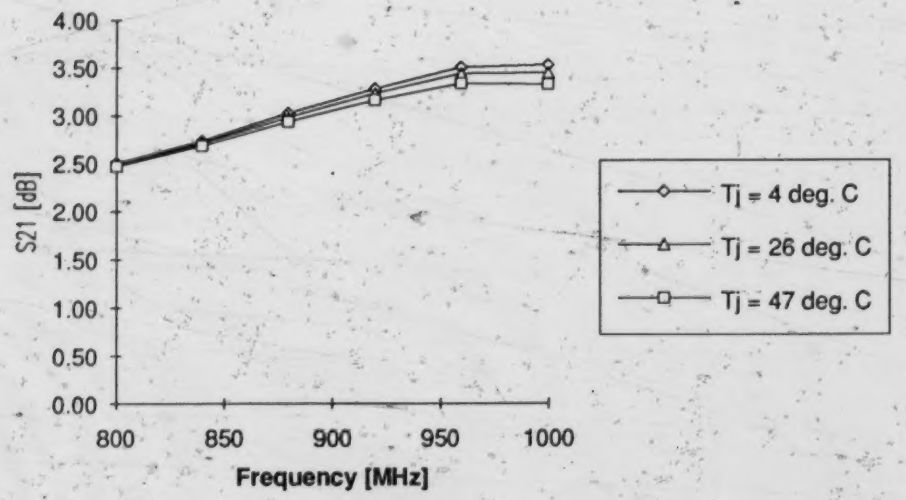


Figure 3.12 S_{21} versus Junction Temperature

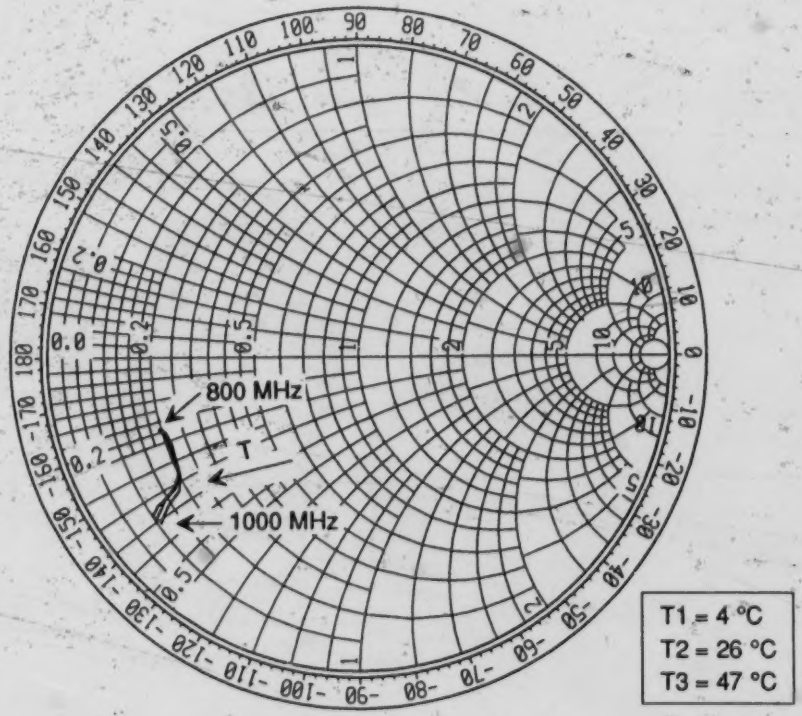


Figure 3.13 S_{22} versus Junction Temperature

characteristic versus temperature at a given frequency. The output parasitic network can desensitize the measured gain to temperature variations, if the active device's output impedance changes significantly with temperature. However, the small-signal output resistance has been shown to be virtually independent of junction temperature [22]. As well, the base-collector junction capacitance is only a weak function of temperature, as discussed in Section 3.2.4.1. Significant variations in S_{21} with junction temperature were not observed, but were also in the same range as the measurement accuracy provided by the network analyzer (as for S_{11} and S_{22}).

The conclusion to be drawn from these measurements is that the variation in τ_F with junction temperature cannot be determined accurately from small-signal S-parameter measurements. However, the variation of τ_F has very little effect on the transistor terminal characteristics. Therefore, the value determined previously at room temperature was used for the large-signal model, for all junction temperatures (see Chapter 6).

3.3 Parasitic Network Development

Package parasitics often assume a dominant role in the operation of RF transistors [14]. The complete transistor model consists of the G-P model for the intrinsic transistor, and a network of lumped components representing the parasitics. One of the primary difficulties in characterizing parasitic effects is in choosing the topology of the equivalent network. Some parasitics may be accurately represented by lumped elements (e.g. lead inductance), while others are more distributed in nature. Only lumped elements are used for the network, and distributed effects are represented by multiple LC sections.

3.3.1 Characterization Methods

The selection of a model topology for the BLV93 is difficult, particularly when the internal device topology is considered. Inter-transistor parasitics are ignored as the composite device is modeled as a single transistor. Initially, a general model (network topology) is assumed which includes lead inductances, and capacitances between the device terminals. The dominant parasitic components are identified during the characterization process, which allows simplification of the model.

Values of the dominant parasitic elements can be determined using various methods:

1. Measure the dimensions of bond wires, distances between various critical points on the device, etc., and calculate element values. This method can produce accurate results, but measurements of the microscopic dimensions in the transistor package were not possible.
2. Perform measurements on packages with a bonded transistor which is no longer functional (either an open or short circuit). Measurements made on empty packages can be useful to estimate capacitive effects. However, lead inductances and their associated distributed capacitive effects can only be determined from measurements made on a device with all the bond wires intact. This method was not used since packages with non-functional devices were not readily available from the manufacturer, and it was difficult to disable the active devices without damaging the bonding wires.
3. Use an optimization technique and calculate the optimal parasitic element values by matching the response of the model to the measured

device response. This process consists of three main stages. First, a model for the intrinsic transistor is developed using low-frequency measurements. Next, a network topology is chosen, and a composite transistor model is formed by combining this network with the intrinsic transistor model. Finally, high-frequency transistor data is measured, and an optimization program finds the optimal network element values by equating the measured and calculated transistor response.

The optimization method can be used with standard devices and provides a convenient method of investigating the effects of various parasitic network topologies. The entire procedure, as outlined above, is repeated for measurements obtained at several operating points. This ensures that the calculated parasitic element values correspond to real physical quantities, and do not represent arbitrary solutions to the mathematically-stated problem. When the calculated element values are the "real" values, they should be the same for all operating points. However, deviations between the calculated element values for different operating conditions do not necessarily indicate that arbitrary element values have been calculated. The success of the optimization process is a function of the optimization algorithm complexity, the accuracy of the intrinsic transistor model, and the topology of the parasitic network.

3.3.2 Representation of the Transistor Chip

An important part of the optimization procedure is the determination of the intrinsic transistor model. The microwave circuit analysis program C/NL (used to optimize the parasitic network) does not provide a bipolar transistor model. Instead, the BLV93 must be represented as a two-port network

described by an S-parameter file, or as an equivalent circuit consisting of passive elements and dependent sources.

Both of the above representations were used to characterize the transistor. In the first method, previously extracted DC and AC parameters are combined to form a complete, low-frequency SPICE model. An AC analysis technique using PSpice [23] is used to generate the transistor's S-parameters at a given operating point over the desired frequency range. As discussed in Section 3.1, there are various difficulties in determining accurate DC and AC model parameters. Hence, the accuracy of this method is uncertain until the computed transistor operation is compared to measured data.

The second method involves finding a relatively simple, small-signal hybrid-π model, as shown in Figure 3.11, which corresponds to the measured low-frequency transistor response. An AC PSpice analysis is combined with previously determined DC and AC model parameters to generate the initial values of the small-signal hybrid-π model parameters.

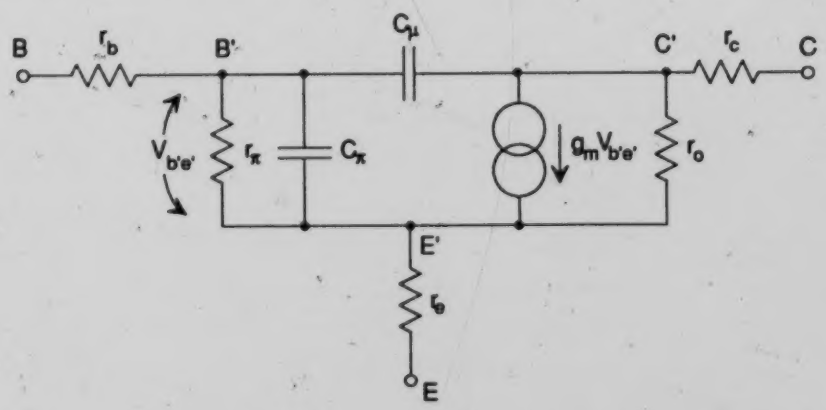


Figure 3.14 Small-signal Hybrid-π Model

Having determined the approximate small-signal model for the transistor chip (parasitics are negligible at low frequencies), the C/NL optimizer (see

Appendix B) is used fine-tune the values to obtain the best correspondence between the measured and calculated transistor characteristics.

The optimizer determines the parameter values by minimizing a performance function, PF. These values depend on the form of the performance function and the transistor model. A convenient performance function for use with an RF transistor is:

$$PF = \frac{1}{N} \sum_{n=1}^{N} \sum_{i=1}^{2} \sum_{j=1}^{2} \left[W_{|S_{ij}|} \underbrace{\left(|S_{ij(c)}| - |S_{ij(m)}| \right)^2}_{\text{(magnitude errors)}} + W_{<S_{ij}} \underbrace{\left(<S_{ij(c)} - <S_{ij(m)} \right)^2}_{\text{(phase errors)}} \right] \quad (3.7)$$

where (c) and (m) denote calculated and measured values of the S-parameters, respectively, and $<S_{ij}$ indicates the angle of S_{ij}. Each of the four S-parameters has a separate weighting function for its magnitude and phase, as indicated in (3.7). These are selected to obtain the best fit with a minimal number of optimization cycles.

Small-signal S-parameters were measured from 300 kHz to 1.3 MHz with the transistor biased for class A operation. Measurements were made at three operating points; V_C = 12.5 V, and I_C = 50, 100, and 250 mA.

The measured value of S_{12}, the reverse transmission coefficient, was observed to be very small (approximately 10^{-4}). This characteristic enables the optimization process to be performed in several runs, each of which determines a separate portion of the circuit. In the first run, S_{11} is fit to the measured data by setting the S_{12}, S_{21}, and S_{22} weighting functions to zero. Values of the input parameters are obtained assuming C_μ to be approximately zero. Next, S_{22} is fitted to determine values for the output circuit. Finally, the element values from the first two runs are adjusted to provide the best fit for S_{11}, S_{21}, and S_{22}.

Neglecting S_{12} (i.e. $W_{|S12|} = W_{<S12} = 0$), magnitude errors of < 4% and phase errors of < 5° were obtained for S_{11}, S_{21}, and S_{22} (for V_C = 12.5 V,

I_C = 100mA). While the accuracy of these results is satisfactory, the low-frequency characterization is unable to resolve all component values. For example, since C_π is in the pF range, its impedance is very large compared to r_π at low frequencies. When C_π is changed from 1pF to 100pF, the model elements and simulation accuracy remain essentially constant. Therefore, accurate values are only obtained for the frequency-independent parameters, using the low-frequency optimization procedure. Previously discussed AC measurements must be used to provide estimates of the transistor's capacitive elements, as these are dominant at high frequencies.

3.3.3 Parasitic Network Topology

The structure of the BLV93 transistor is relatively complex, and few assumptions regarding the topology of the network can be made by examining the device. A very general parasitic network was assumed, as shown in Figure 3.12. The LC network is provided at the input to account for the transistor's input matching network.

3.3.4 High-Frequency S-parameter Measurements

Small-signal S-parameters measured in the RF frequency range (600 MHz to 1200 MHz) are required for the final phase of the optimization process. Again, the transistor was biased for class A operation, and measurements were made at three operating points (I_C = 50, 100, and 250 mA at V_C = 12.5 V).

A full two-port calibration was performed on the network analyzer (see Section 3.1.1.2) to translate the measurement reference plane to the transistor terminals. Input power levels were checked during the small-signal testing to ensure that the results were independent of the power level (linear operation).

3.3.5 Parasitic Network Optimization

An optimization technique similar to that used for the development of the intrinsic transistor chip model is used for the characterization of the parasitic network. As discussed earlier, the procedure must be repeated for several DC operating points to ensure that the element values are unique, and do not represent arbitrary solutions to the mathematical problem. Repeating the procedure not only assures correct parasitic element values, but it also provides a indication of the accuracy of the assumed network topology.

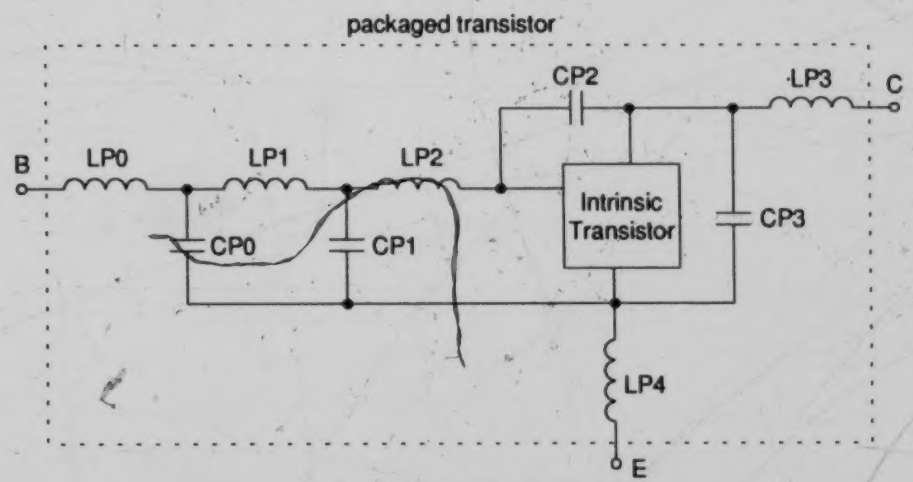


Figure 3.15 BLV93 Model with General Parasitic Network

3.3.5.1 *Characterization of the BLV93 Parasitic Network*

The performance function of (3.7) was used for the optimization of the parasitic network. The $S_{12} \approx 0$ simplification could not be used at high frequencies, so the optimization was performed in a single step (all weighting functions are non-zero in the performance function). All parasitic capacitances are initially set to 1 pF (except CP1 which is expected to be about 75 pF from

the low frequency junction capacitance measurements), and lead inductances are set to 1 nH.

Initially, the two-port network model was used to represent the intrinsic transistor. The optimizer was unable to find a satisfactory solution for the parasitic network, however, even when no restrictions were placed on the variable network elements (the default variable range in C\NL is 10^{-18} to 10^{+10}). Only single S-parameter solutions could be obtained by manipulating the performance function. For example, an excellent fit for S_{11} was obtained by setting the weighting functions for the other S-parameters to zero. However, when a second S-parameter was introduced in the optimization, the accuracy of the fit was severely degraded.

The discrete hybrid-π model was also used to represent to the instrinsic transistor. Initially, the hybrid-π elements values, obtained as described above, were allowed to vary by ±10%, and the variation of the parasitic network elements were unrestricted. A solution was obtained for the I_C = 100 mA case which provided a 10% magnitude accuracy, and a 10° phase accuracy, for all S-parameters except $\angle S_{12}$. This is satisfactory, especially considering the simplifications which were used thus far in the model development.

This procedure was repeated for the two other operating points, with the starting parasitic network values being those determined for the I_C = 100 mA case. Initially, the variable restrictions were kept the same as in the previous case. The optimizer was able to find solutions which provided similar accuracy to the previous case; many of the network elements, however, varied by up to an order of magnitude. After optimization had been completed for the three operating points, the parameters were averaged, and the S-parameters were re-computed. This process was unsuccessful, as significant deviations between the measured and calculated data were observed in all three cases.

The entire procedure was repeated with all variable parameters restricted to ±10% deviations from their initial values. The results showed that at the end of an optimization run, most of the variables were at the limits, and further improvements could only be obtained by relaxing the limitations. Averaging produced results of similar accuracy to the previous case.

Finally, the optimal parasitic network values for the 100 mA case (middle value) were fixed, and the optimization was repeated for the hybrid-π parameters only. It was speculated that the variations observed in the parasitic element values were a result of the optimizer compensating for errors in the hybrid-π model. However, the results of this procedure were unsatisfactory.

After several iterations of the above procedures, it was concluded that it is necessary for each operating point to have its own parasitic element values. While this is not exactly the desired result, the optimization procedure produced three useful results:

1. Many elements were found to be negligible (such as emitter and collector inductances), enabling simplification of the network topology.
2. A range of values was determined for the parasitic elements
3. Large parasitics which were indicated by the low-frequency junction capacitance measurements were confirmed.

The values of the parasitic elements cannot be uniquely determined using this procedure. The method provides limited information about the network topology, and enables fine-tuning of the parasitic network during the large-signal simulation phase by providing a range of element values. The final simplified model topology is shown in Figure 3.13.

3.3.5.2 *Difficulties with the Optimization Technique*

The success of the optimization technique is limited by several factors. The BLV93 is a relatively complex device, and simplification of the parasitic network and inter-transistor interactions inevitably causes model inaccuracies. Even if the device consisted of a single transistor, the simple hybrid-π model would provide only an approximate description of the transistor operation. Since the low and high-frequency ranges differed by about 3 orders of magnitude, it is anticipated that a model developed for the low-frequency range may not provide an accurate representation at the high-frequency range. Previous works have described methods of enhancing the hybrid-π model for use at RF and microwave frequencies [24]. However, the added complexity was found to complicate the problem while providing little improvement in the model accuracy.

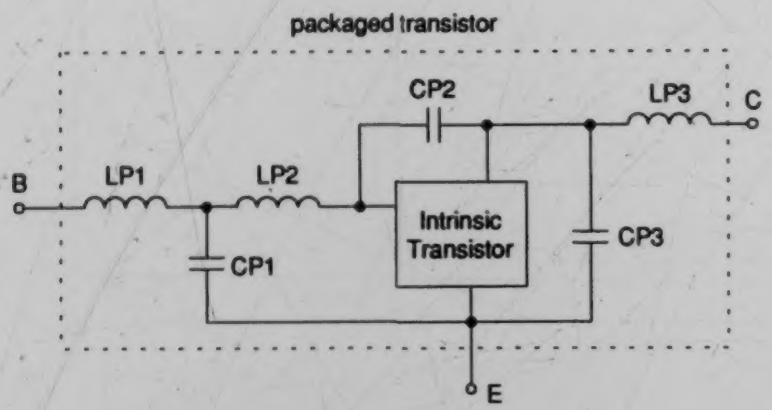


Figure 3.16 Final Parasitic Network

In addition to the simplifications used in the characterization of the device, there are several difficulties with the simulation procedure which contribute to its limited success. The optimizer minimizes the performance

function as previously outlined. However, if a satisfactory starting point is not presented to the optimizer, the determined minima may only be a local minima. Also, the success of the optimization was found to be highly dependent on the relative weights on the various terms. The weights were initially selected so that the magnitude and phase limits of each S-parameter was approximately 5% and 3°, respectively. A systematic procedure could not be determined to provide the required weighting function values in order to produce consistent results.

Finally, errors present in the measured results create problems when trying to fit the measured and modeled S-parameters. Throughout the procedure, the measured values are assumed to be correct. A careful calibration procedure was followed to minimized measurement errors, but precise standards from the calibration kit could not be used to calibrate the custom test fixture.

The interaction of the above error sources is very complex. While an attempt is made to minimized each source, it is uncertain how the errors combine to affect the accuracy of the characterization process. Although the above discussion seems pessimistic, optimization remains one of the best methods presently available for the characterization of package parasitics. The primary consequence of the error sources is that parasitic network values cannot be determined which are valid at all frequencies and for all transistor operating conditions. However, the procedure is able to provide accurate results when limits are placed on these operating conditions.

4. EXPERIMENTAL CLASS B RF POWER AMPLIFIER

An 850 MHz tuned class B amplifier was used to obtain data to verify the accuracy of the large-signal RF transistor model. This chapter describes the experimental amplifier circuit and the models used for its simulation in the time domain.

A brief overview of tuned amplifiers is given, indicating that single-ended class B operation can be considered as a special case of class C operation. The experimental circuit is presented, and its operation and tuning capabilities are described.

An accurate amplifier circuit model is very important in the development of the transistor model. This circuit model ensures that discrepancies between the measured and simulated amplifier performance may be isolated and attributed to inaccuracies in the transistor model. Two models are introduced for representation of the amplifier: the equivalent circuit model consisting of only lumped elements, and the transmission line model which uses a combination of distributed and lumped components. A method is presented for determining the model parameters using small-signal S-parameter measurements and optimization.

4.1 Basic Features of Tuned Amplifiers

Tuned power amplifiers provide efficient amplification of FM and PM signals for cellular radio applications. These amplifiers are more efficient than linear class A amplifiers during normal operation, and they do not dissipate power in the absence of an input signal.

The class B amplifier topology, shown in Figure 4.1, is similar to that of a class C amplifier. Input and output matching circuits transform the low transistor impedances to values which are compatible with the source and load impedances. Blocking capacitors are used to isolate the RF source and load from the DC supply voltages. In the class B configuration, the base is connected via an RF choke to ground, rather than to a negative supply voltage, as in the class C configuration. Therefore, the conduction angle of the self-biased class B amplifier is 180° (neglecting the non-ideal switching characteristic of the transistor). Both class B and class C configurations require a resonant output circuit to supply the negative portion of the RF cycle, when the transistor does not conduct.

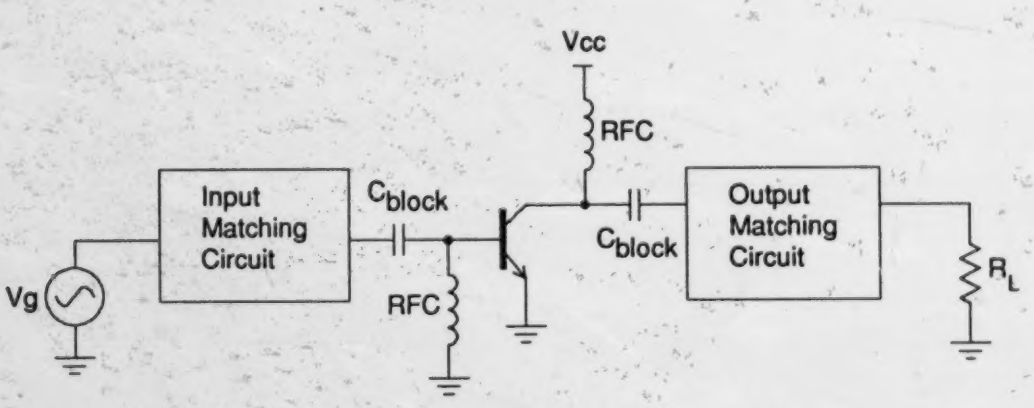


Figure 4.1 Block Diagram of a Class B Tuned Amplifier

The efficiency of the class B amplifier is obtained using theoretical relationships derived for class C amplifiers, for a conduction angle of 180°. This calculation indicates a maximum collector efficiency of 78.5%, which is consistent with the result for a class B push-pull configuration [25,26]. The theoretical efficiency of the ideal class C amplifier approaches 100% as the conduction angle is decreased toward zero. As the efficiency is increased,

however, the amplifier requires a higher peak collector current in order to maintain a constant output power, and a larger reverse base voltage to reduce the conduction angle, which reduces transistor reliability. Therefore, class B operation is better suited for single transistor amplifiers, where the maximum output power is often limited by the maximum collector current rating of the transistor.

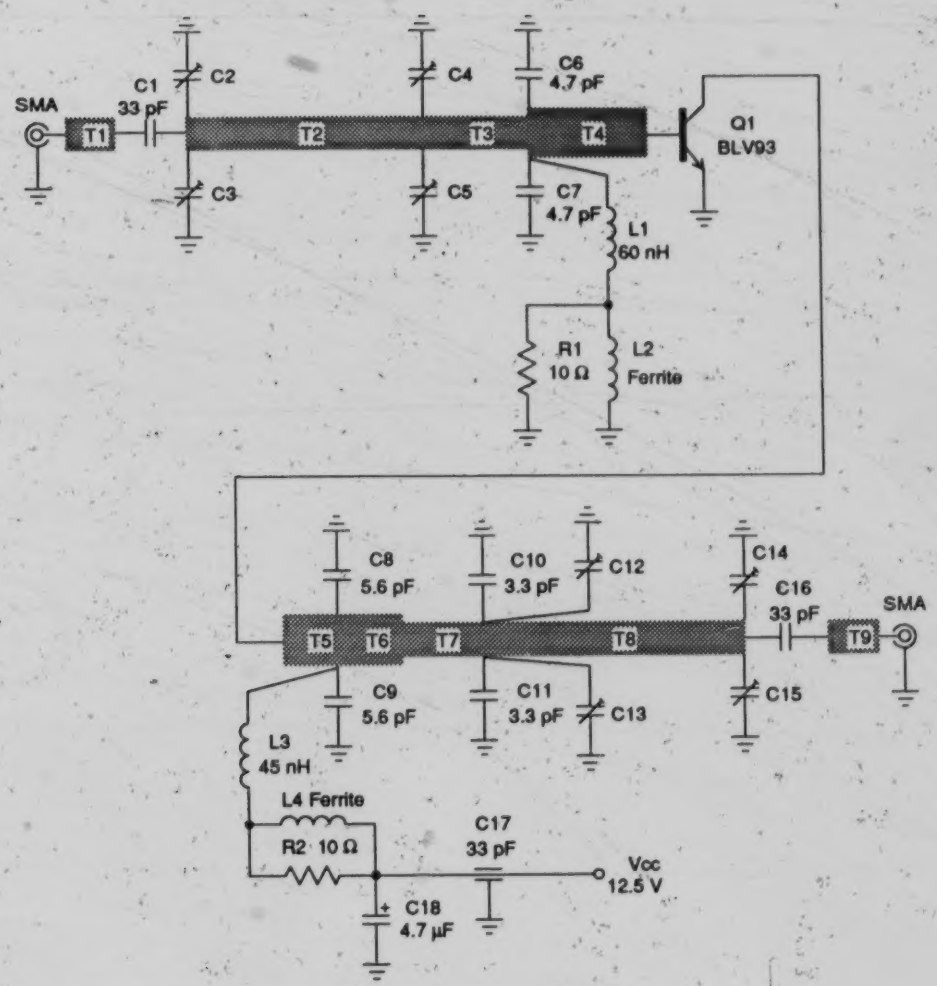
4.2 Experimental Amplifier

The 850 MHz class B amplifier circuit is shown in Figure 4.2. This circuit is based on the test amplifier design given in the transistor data sheet (see Appendix A). Some changes were made to the design to enable implementation of the circuit using a fiberglass PC board ($\varepsilon_r = 4.8$, instead of a P.T.F.E. dielectric, $\varepsilon_r = 2.2$, as specified).

4.2.1 Circuit Description

The amplifier was tuned by adjusting the eight trimmer capacitors. A double stub matching circuit, with a minimal forbidden region, was implemented by separating the trimmer capacitors by a quarter-wave transmission line (in both input and output circuits). The additional transmission lines provide initial transformation of the low transistor impedances, and compensate for bias circuit reactances.

Adjustment of the trimmer capacitors changes the source and load impedances seen by the transistor. A numerical analysis was used to determine the ideal range of values of these impedances, and the result is shown in Figure 4.3 for the input circuit. The output circuit tuning capability is



All trimmer capacitors = 1.5 to 4.5 pF

L1 = 4 turns of closely wound enamelled copper wire (0.4 mm)
internal diameter = 3 mm, leads 2 x 5 mm
L3 = 4 turns of enameled copper wire (1.0 mm)
length = 6 mm, internal diameter = 4 mm, leads 2 x 5 mm

T1 = 50 Ω stripline (25.0 x 2.9 mm)
T2 = 50 Ω stripline (21.1 x 2.9 mm)
T3 = 50 Ω stripline (4.4 x 2.9 mm)
T4 = 42.7 Ω stripline (9.7 x 3.6 mm)
T5 = 42.7 Ω stripline (3.3 x 3.6 mm)
T6 = 42.7 Ω stripline (3.4 x 3.6 mm)
T7 = 50 Ω stripline (8.0 x 2.9 mm)
T8 = 50 Ω stripline (21.1 x 2.9 mm)
T9 = 50 Ω stripline (25.0 x 2.9 mm)

T1 to T9 are microstrip lines on a double-sided PC board with fiberglass dielectric (ε_r = 4.8), thickness = 1.6 mm.

Figure 4.2 850 MHz Class B Amplifier Circuit

similar to that of the input circuit, except that the impedance variation is provided about the (15 + j0)Ω point.

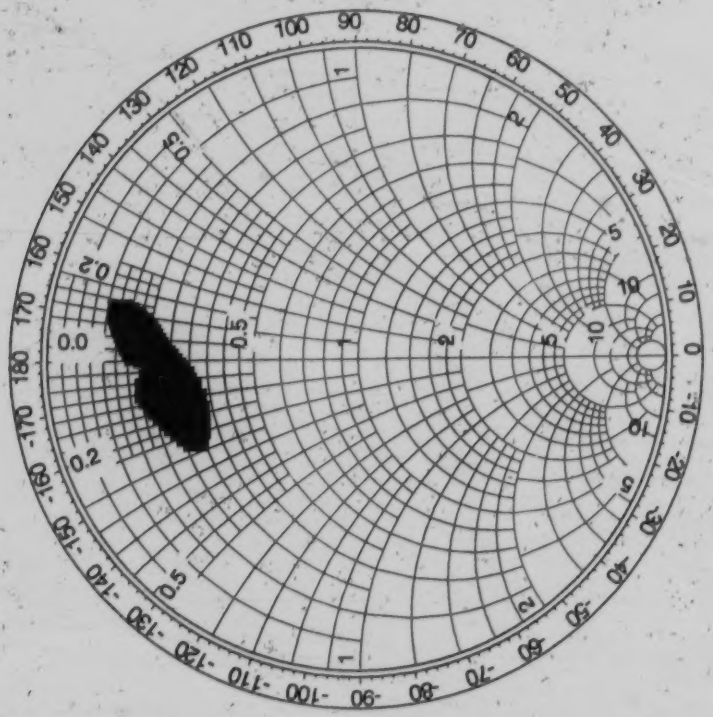


Figure 4.3 Input Circuit Tuning Capability (Normalized with respect to 50 Ω)

4.2.2 Amplifier Construction

The use of proper fabrication techniques and special circuit components is essential to ensure that the RF amplifier operates as expected. This section discusses various practical considerations in building the RF power amplifier.

A diagram of the amplifier assembly is given in Figure 4.4. The circuit is mounted in an aluminum enclosure which provides RF shielding, and ensures stable amplifier operation.

DC base and collector bias voltages are provided through RF chokes. These are constructed using several turns of enamelled wire, as specified in Appendix A. Passive networks provide additional RF filtering in the bias circuits. Small-value resistors (R1 and R2) must be included to reduce the Q of the bias circuits, and avoid amplifier oscillations. A feed-through capacitor, C17, is used in the collector bias circuit to ensure that RF energy is only transferred through the input and output connectors.

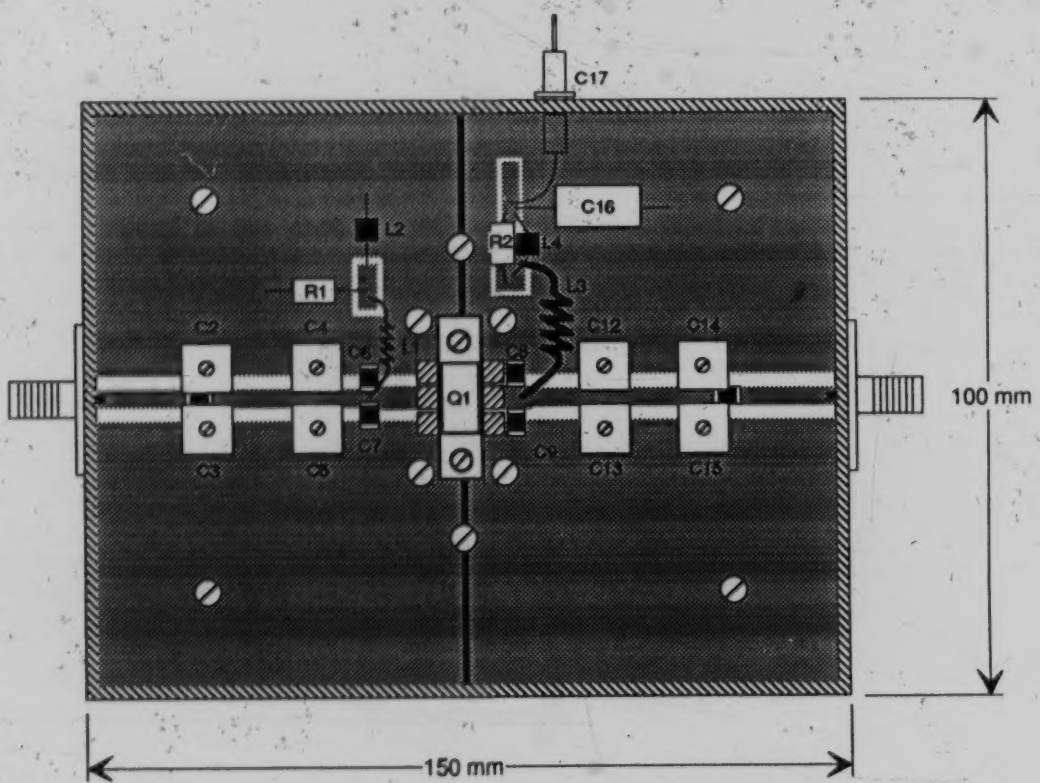


Figure 4.4 Class B Amplifier Assembly

Trimmer capacitors enable precise matching of the low-impedance transistor to the RF source and load. High-quality P.T.F.E. (Teflon) dielectric fixed and trimmer capacitors are required in the input and output circuits to

minimize dielectric losses. Since these components are subjected to relatively high power levels, moderately lossy dielectrics will dissipate sufficient power to exceed the capacitor's maximum power rating. This eventually destroys the capacitor, and often the RF transistor, as the process usually results in large currents flowing through the transistor.

Trimmer capacitors are connected to a ground plane on top of the circuit board. A low inductance path is provided between the top and bottom ground planes using metal screws and copper straps around the circuit board. Additional screws, and copper straps at the transistor slot provide direct contact between the transistor's emitter contacts and the ground plane. This is necessary to ensure amplifier stability, and to provide maximum RF gain.

4.2.3 Amplifier Tuning

After constructing the amplifier, it was found that initial tuning was difficult and could not be achieved by simply monitoring the output power. Instead, an experimental setup was used to monitor the forward and reflected power at the amplifier ports (see Figure 4.5). The output waveform was also monitored with an oscilloscope to ensure stable amplifier operation.

After determining the nominal trimmer capacitor settings, additional tuning was performed to simultaneously maximize the output power (gain) and minimize the DC collector current (input power). The complex interaction between the input and output circuits prevented the determination of a systematic method for obtaining optimal amplifier performance. Therefore, the final amplifier settings do not necessarily provide the optimal amplifier performance. This does not present a serious problem, since an optimal amplifier is not required for the modeling project.

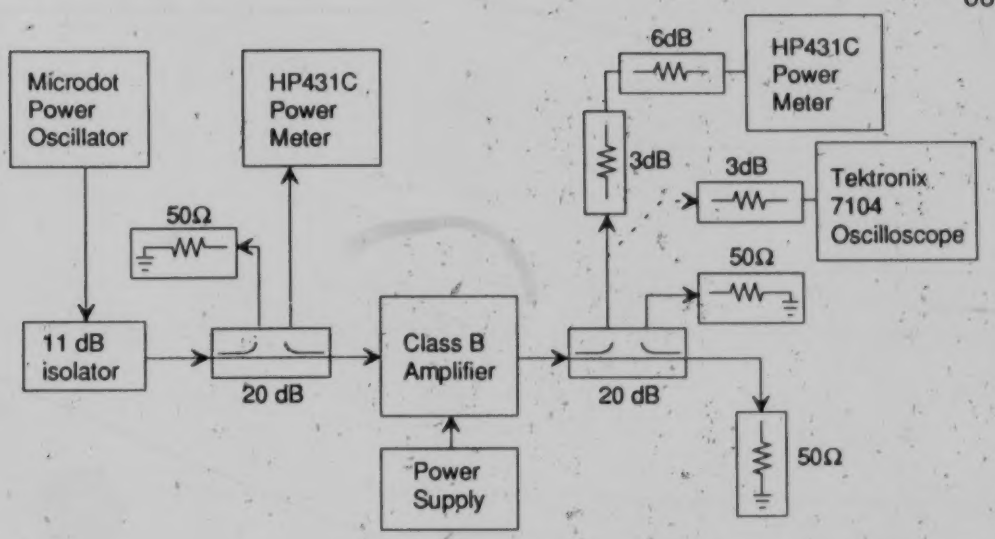


Figure 4.5 Experimental Setup for Amplifier Tuning

4.3 Amplifier Circuit Models

Accurate amplifier circuit models are important for the development of the RF transistor model. Although the input and output matching circuits contain distributed circuit elements, any circuit model which accurately describes the impedances seen at the transistor terminals, over a given frequency range, can be used. Furthermore, since the amplifier is driven by an 850 MHz CW source, the amplifier circuit models need only be accurate at the fundamental and first few harmonic frequencies.

The above operating constraints suggest that an equivalent circuit, consisting of lumped passive components, is satisfactory to model the input and output matching circuits. This method has been used successfully for the simulation of a large-signal microwave amplifier [14]. This work indicates that circuit modifications are required to obtain efficient simulation results.

The topology of the equivalent circuit, and its component values tend to introduce large time constants into the circuit. Therefore, a significant amount of computer time is necessary to reach steady-state operation. This time can be reduced by altering the topology of the equivalent network, and removing small-valued components in the transistor's parasitic network. Altering the network topology usually results in reduced model accuracy at the second and higher harmonic frequencies [14,27]. This is justified when the transistor operates close to its f_T, since harmonic generation is negligible. While the BLV93 does not operate close to its f_T in the 850 MHz amplifier ($f_T \approx 4$ GHz), large-value package parasitics tend to prevent harmonics from reaching the amplifier circuits.

Another alternative for modeling the amplifier circuits is to develop distributed circuit models. These combine ideal or microstrip transmission lines with lumped elements to represent the circuit as given in the schematic. These models are not very efficient, but are convenient to use and provide an accurate description of the amplifier circuits over a wide frequency range. Therefore, the same models can be used to analyze the amplifier at various excitation frequencies.

The use of microstrip transmission line models is desirable for the circuit model, since they account for dielectric losses, and non-ideal dispersion effects. These models are best described in the frequency domain, however, and are not available for transient analysis in PSpice. Instead, ideal transmission models must be used. Losses are represented by dividing the transmission lines into small sections and inserting lumped resistances. While this method provides satisfactory results, simulation times are increased significantly when multiple short length transmission lines are used.

4.4 Amplifier Circuit Characterization

Equivalent circuit and transmission line models were both synthesized to correspond to the measured response of the amplifier circuits at the transistor terminals. After the measured response was obtained, optimization techniques were implemented to determine the values of the circuit components and transmission line parameters.

4.4.1 Network Impedance Measurements

Accurate source and load impedance data, as seen from the transistor terminals, are required to determine accurate models for the amplifier circuits. These data were obtained with the HP8753A network analyzer and HP85046A S-parameter test set. A calibration procedure was used to ensure that the measured data corresponded to the impedance of the amplifier under test. This is an important consideration in high-frequency measurements, since the desired data are significantly affected by the intermediate network of transmission lines and connectors between the amplifier circuit and the network analyzer.

4.4.1.1 *Measurement Procedure*

As shown in Figure 4.4, the amplifier's input and output matching circuits reside on separate circuit boards. After the amplifier was tuned, the output circuit was measured by removing the transistor and the input circuit. A circuit board with a single, 50 Ω transmission line was then inserted to connect the network analyzer to the output matching circuit (at the transistor terminal location), as shown in Figure 4.6.

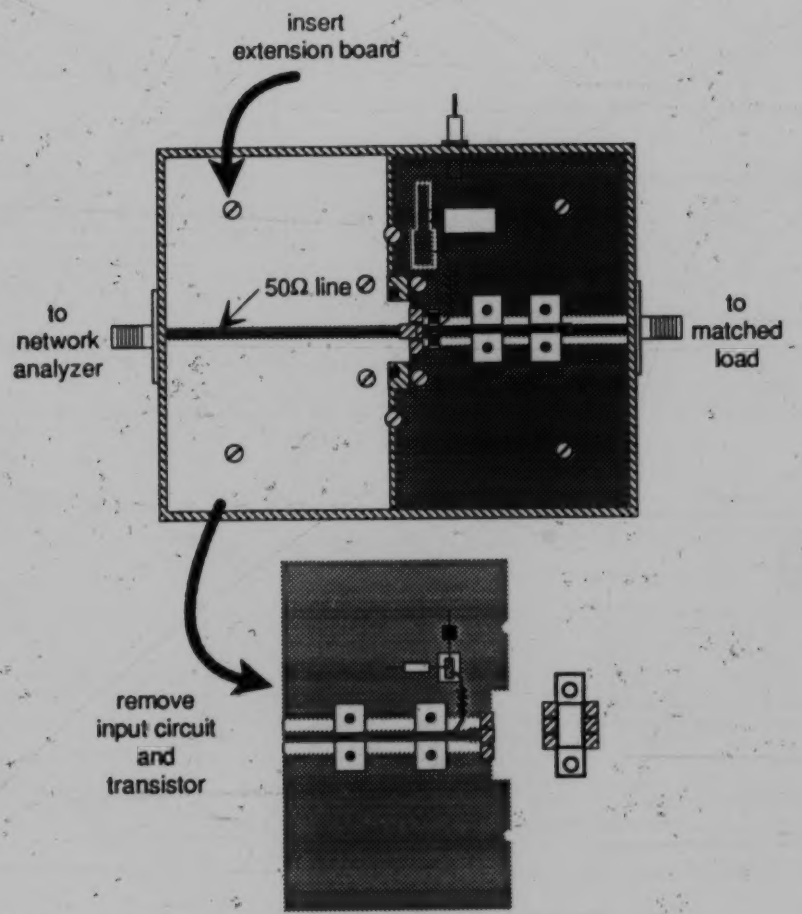


Figure 4.6 Network Impedance Measurement Assembly

A gold tab at the end of the 50 Ω line was pressed against the amplifier circuit under test to provide the connection between the extension board and the output circuit. The effect of the discontinuity at this junction is neglected, since it is approximately the same as that of the transistor mounted in the amplifier.

Tests were performed to determine the effect of the output termination on the measured impedance seen at the amplifier's transistor terminal. During tuning, the output was connected to a matched load and a power meter (via a

directional coupler) for monitoring forward power. This same configuration should be connected to ensure that the measured load impedance is the same as seen by the transistor during the tuning process. After measuring the impedance with the output connected to the test equipment, the process was repeated using a matched load at the output. The measurements were insensitive to this change, and subsequent impedance data were obtained by terminating the output with the matched load. This is not only convenient, but ensures consistent results as the matched load only introduces a single discontinuity at the output.

The input reflection coefficient (input impedance) was measured from 500 MHz to 1.8 GHz. This is a sufficient range to measure the impedance at the fundamental and second harmonic frequencies for the 800 to 900 MHz cellular radio band. Accurate measurements at higher frequencies were not possible, since the calibration was observed to be marginal at frequencies exceeding 2 GHz (see Section 4.4.1.2).

After completing the output circuit measurements, the above process was repeated for the input circuit.

4.4.1.2 *Calibration*

As was discussed in Chapter 3, calibration is necessary to translate the reference plane of the network analyzer from its front panel connectors to the desired measurement location. In addition to providing this function, the built-in calibration routine corrects for connector discontinuities and non-ideal frequency response in the impedance measurements.

Since the transistor terminals are not connectorized, calibration cannot be achieved using the network analyzer's calibration kit. Thus, another set of "standards" were made to provide approximate calibration of the network

analyzer. Three circuit boards provide open, short, and 50 Ω terminations which appear at precisely the same location as the input terminals of the circuit being measured. These boards are slightly longer than the extension board, and the matching circuit under test must be removed for calibration (preferably the calibration procedure is performed prior to tuning the amplifier circuits). An abbreviated calibration sequence (full 1-port calibration) was used for these measurements, since only reflection measurements (input impedance) are made. The calibration was observed to produce consistent results up to approximately 2 GHz. Above this frequency, the impedances of the "standard" terminations began to deviate from their nominal values. While this may simply represent the actual response of these terminations, the calibration was assumed to be invalid in this region.

A similar calibration procedure was used in measuring the input network. Since the actual input and output circuits were not exactly symmetric, separate "standards" were made to ensure that the terminations appear at precisely the same location as the input terminals of the circuit being measured. Thus, separate calibrations are required for each set of measurements. Even if the matching circuit boards were symmetric and could use the same extension and calibration boards, separate calibrations should be made for the input and output circuit measurements. This avoids errors due to the change in orientation of various components inside the circuit enclosure (e.g. feedthrough capacitors and mounting hardware).

Since the input and output circuits contain trimmer capacitors, the circuit boards must be removed and handled carefully to avoid altering the component settings. After performing the impedance measurements, the amplifier was reassembled to verify that the gain and efficiency were as previously measured.

4.4.2 Equivalent Circuit Model

The measurement system described above was first used to characterize the output tuned circuit. Impedance measurements at the fundamental and second-harmonic frequencies indicated that the output circuit could be represented by a parallel tank circuit connected to the transistor via a series inductor and blocking capacitor.

Component values were determined by entering the circuit topology and the measured S-parameter data into the optimization program C/NL. Optimization of the input reflection coefficient is achieved by setting all weighting functions in the performance function (equation 3.7) equal to zero, except for those corresponding to S_{11}.

The calculated component values provide 4% magnitude accuracy, and 6° phase accuracy in the input impedance at the first and second harmonic frequencies. The circuit topology and component values are shown in Figure 4.7.

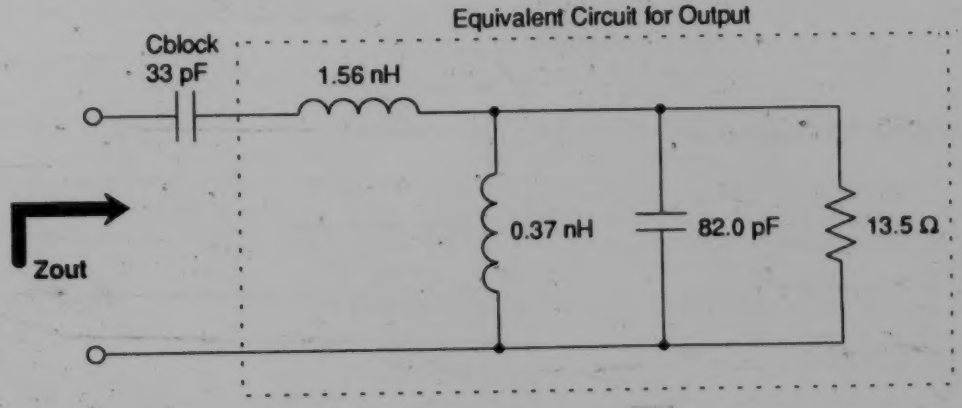


Figure 4.7 Equivalent Circuit Model for Amplifier Output Circuit

Additional analysis was performed to determine the response of the network over the measured frequency range. These results, shown in Figure

4.8, indicate that the form of the response is not correct over the full frequency range. However, the calculated impedance is within 5% of measured at the fundamental and second harmonic frequency points. The circuit is inductive at high frequencies, which is consistent with measurements (even though the accuracy of the calibration is not precise above 2 GHz, an inductive response is indicated for the output circuit at high frequencies).

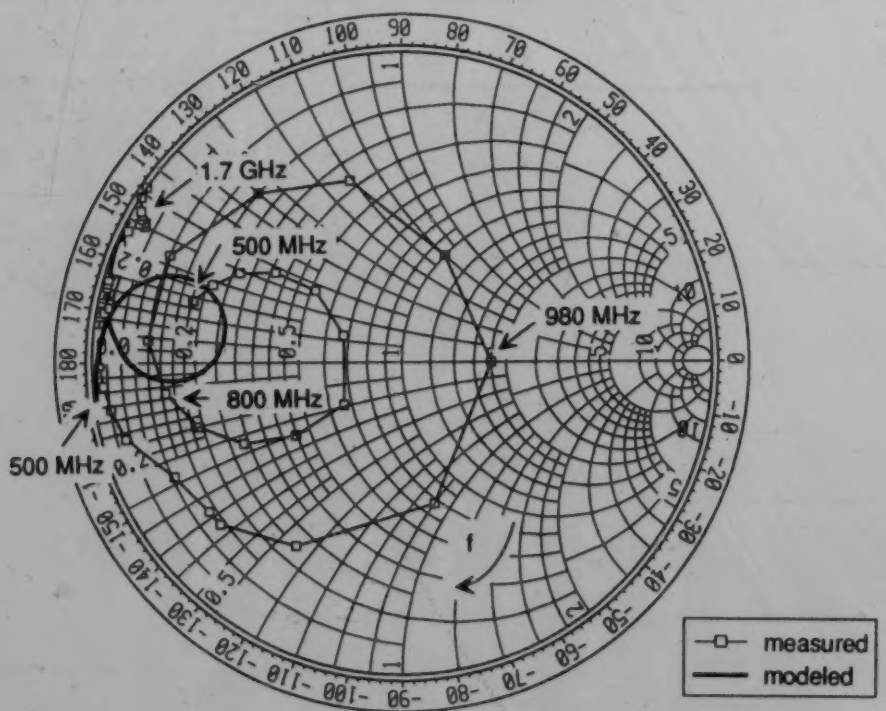


Figure 4.8 Input Impedance of Output Matching Circuit

A preliminary time domain analysis was performed to investigate the effect of the component values on the simulation efficiency. The model parameters and the parasitic network, as specified in Chapter 3, were used to represent the transistor. The input circuit was not included, and the base was driven by an ideal voltage source.

The simulation efficiency was not determined, as PSpice was unable to find a stable operating point using the equivalent output circuit model (i.e., the simulated circuit oscillated). The output circuit and the collector bias network combine to create a resonant circuit which peaks at approximately 40 MHz, where the DC collector current was observed to oscillate.

The circuit was stabilized by adjusting the resistance parameters in the transistor model. In addition to providing poor simulation accuracy, this solution is undesirable because the physical significance of the model parameters is lost. Several changes were made to the circuit topology, but a satisfactory solution was not obtained. It is apparent that the interaction of the amplifier circuit and the transistor's parasitic network is complex, and a considerable effort would be required to obtain a stable amplifier model.

Due to these difficulties, an equivalent circuit model was not synthesized for the input circuit. Instead, a distributed model was investigated, as outlined in the following section.

4.4.3 Transmission Line Model

The input and output matching networks consist of a combination of lumped and distributed circuits, and are best described by a model which includes microstrip or transmission line models. Since PSpice does not provide non-ideal microstrip models, ideal transmission lines must be used and losses represented by passive components (if necessary).

C/NL provides models for ideal transmission lines and microstrip circuits. Initial model development proceeded using the microstrip model, since it includes non-ideal loss and frequency response characteristics. After the microstrip model has been developed, it is converted to include ideal transmission lines, so that it will be suitable for PSpice analysis.

The microstrip model parameters were allowed to vary by ±10% from their ideal design values. This fine-tuning is used to compensate for non-ideal transmission line behavior which is a result of several factors:

1. Circuit dimensions which are slightly inaccurate due to the PCB fabrication process.
2. The presence of the top-side ground plane and enclosure walls, which tend to reduce the characteristic impedance of the microstrip lines.
3. Discontinuities at the transistor device terminals.

In addition to the amplifier circuit topology, a LC network was included to account for discontinuities at the source and load connectors [28]. The optimizer was able to find solutions for both input and output circuits in which the microstrip parameters were nearly ideal, and the trimmer capacitances were within their specified range.

As discussed above, the microstrip transmission lines must be replaced by equivalent ideal transmission lines for simulation using PSpice. Initially, each microstrip line was replaced with an ideal transmission line, with the characteristic impedance and electrical length values corresponding to the previously calculated microstrip model. The optimizer adjusts these values to account for non-ideal behavior, as described above.

The resulting model performance was virtually identical to that of the non-ideal microstrip model. Trimmer capacitance values were consistent with the previously calculated values, verifying the physical significance of the model. The results for the measured and modeled input impedances (using the ideal transmission line model) are shown for the input and output networks

in Figures 4.9 and 4.10. The full amplifier model, including the model parameter values, is shown in Figure 4.11.

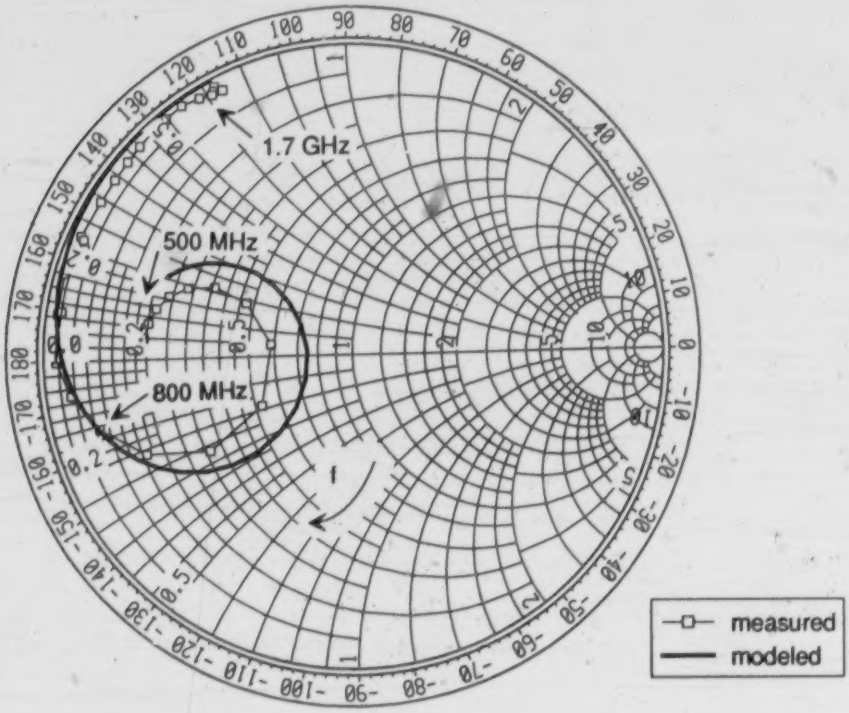


Figure 4.9 Impedance of Input Network at the Transistor Terminal

As in the development of the equivalent circuit model, the amplifier and transistor models were used to perform an initial time domain analysis with PSpice. Unlike the previous case, the circuit was stable over a wide range of input power levels, and steady-state behavior was normally reached within 200 RF cycles.

At low power levels, however, the circuit tends to ring, and the simulation time must be extended to reach steady-state conditions (up to 400 RF cycles are required). While this model is not computationally efficient, it is accurate over the full measured frequency range. Simulation run times are minimized by using dedicated workstations to calculate the amplifier response. The

simulation time was approximately 20 minutes using a SUN SPARCstation 1+ workstation.

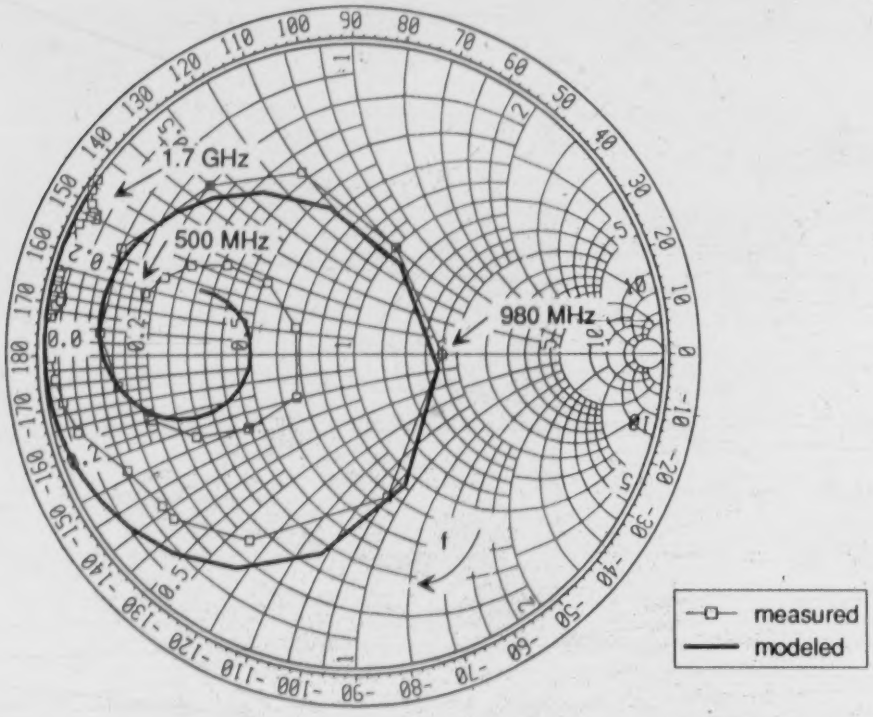


Figure 4.10 Impedance of Output Network at the Transistor Terminal

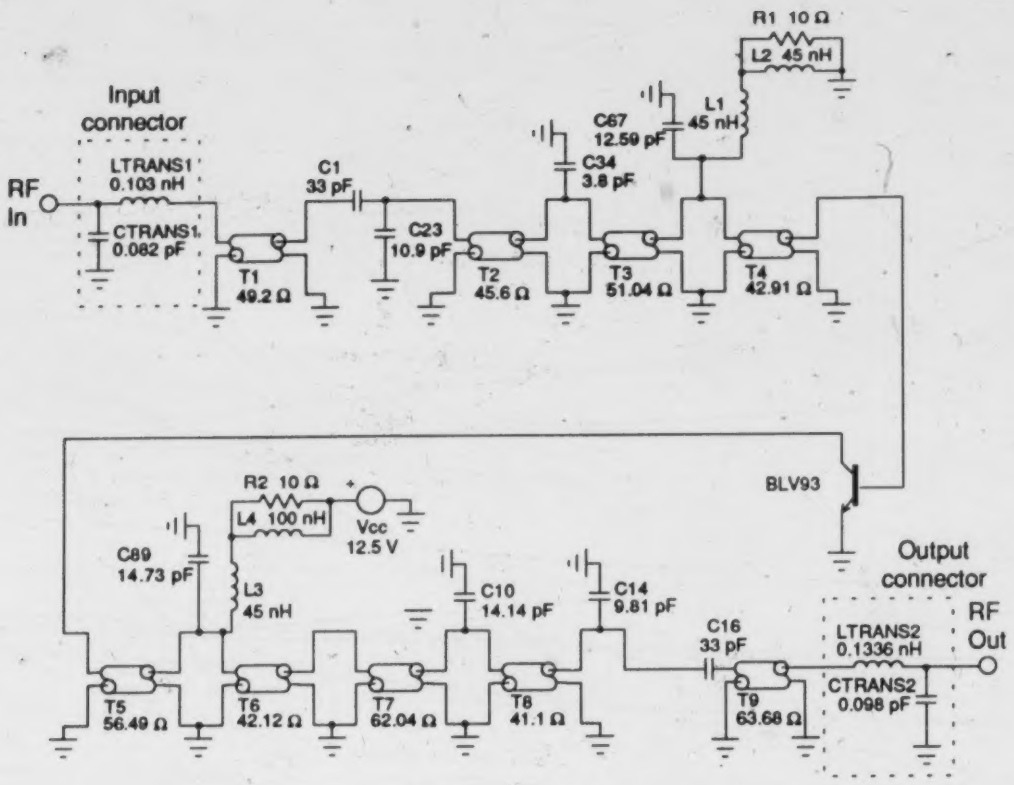


Figure 4.11 Final Amplifier Model using Ideal Transmission Lines

5. TEMPERATURE MEASUREMENT OF BIPOLAR JUNCTION TRANSISTORS

Junction temperature is an important operating parameter for bipolar junction transistors. Several transistor model parameters are strong functions of junction temperature, as shown in Chapter 3. This chapter describes methods of determining the junction temperature of a transistor dissipating relatively large amounts of RF power. These data are used to investigate the effect of junction temperature on the simulation of an RF power amplifier.

5.1 Thermal Resistance Model

Ideally, a complete transistor model should include an algorithm to calculate the junction temperature as a function of operating point and ambient temperature. Theoretically, a thermal resistance model can be used to provide this function. In this model, the flow of heat from the transistor junction to the heatsink is analogous to current flowing through a resistor. The power dissipated in the device flows through a constant thermal resistance, R_θ, between the junction and a reference point (usually the mounting base or heatsink). This causes a temperature difference to develop between the junction and the reference point. The temperature relationship is stated mathematically as :

$$T_j = P_{diss} R_\theta + T_{reference} \qquad (5.1)$$

While this method enables the calculation of junction temperature from the operating point, the computed value is only an estimate of the actual value.

This is a result of two assumptions made in developing the model [29]:

1. Junction temperature is uniform throughout the transistor
2. R_θ is a device constant, independent of the transistor operating conditions.

These assumptions are valid for ideal transistors, however, the thermal resistance of a real transistor is a complex function of chip location and transistor operating conditions. This can be seen by considering a transistor operating at two different operating points and dissipating the same amount of power. For the low-voltage, high-current case, current is distributed relatively evenly throughout the transistor chip. However, in the high-voltage, low-current case, current flow is concentrated in a small region of the device. Therefore, thermal resistance is a function of the power density distribution, and a unique value cannot be defined which is valid for all operating conditions.

The problem is further compounded when considering the case where the transistor's operating point varies continually, as in a pulsed RF power amplifier. Although only an average value of junction temperature is required for the transistor model, a method is not available to determine a meaningful, average thermal resistance value.

The heatflow problem in an RF power transistor is very complex. Due to simplifications which must be made to keep the problem manageable, none of the available models provides an accurate representation of the RF transistor's thermal behavior [30]. This complex behavior was confirmed by preliminary measurements made on the BLV93 transistor. Therefore, no attempt was made to develop a model to predict junction temperature. Instead, accurate

temperature data were measured with the transistor operating in its normal class B configuration.

5.2 General Methods of Measuring Junction Temperature

In general, there are two types of method for determining the junction temperature of a transistor [31]. In the first set of methods, junction temperature is determined by observing the exposed semiconductor chip. Examples of this method are infrared microradiometry and thermographic phosphor techniques. These techniques are useful for mapping the temperature distribution of the transistor chip, and for determining the transistor's peak junction temperature. However, the measurements are time consuming, and are only useful for steady-state characterization [29]. In addition, expensive equipment is required to provide accurate control of the thermal environment of the device.

In the second set of methods, junction temperature is determined by measuring a temperature sensitive electrical parameter (TSEP) of the device. Electrical techniques are convenient since normal, packaged devices can be used for testing. However, these methods can only determine the average temperature of the device, and provide no information about the temperature distribution of the transistor chip.

An electrical measurement technique is suitable for determining the average junction temperature of an RF transistor for use in power amplifier simulation. In addition to providing convenient determination of the device's junction temperature, the method is quantitatively accurate for both steady-state and transient conditions [31].

5.3 Electrical Method of Measuring Junction Temperature

Electrical measurement of junction temperature is normally accomplished in two steps. In the calibration step, the selected TSEP is characterized versus junction temperature at a fixed operating point. In the measuring step, the device operates in its normal amplifier configuration, where it experiences self-heating due to internal power dissipation. Junction temperature is determined by interrupting the normal operation, and measuring the TSEP at the operating point used in the calibration step. The corresponding junction temperature is obtained using the measured data from the calibration step.

The method is particularly useful for determining the thermal performance of a transistor operating in a non-ideal amplifier assembly. The method does not assume ideal heatsink characteristics, so it can be used to determine the performance of amplifiers using various heatsink materials and/or designs. Elaborate schemes to provide precise control of the heatsink temperature are unnecessary, since junction temperature is measured directly.

5.3.1 TSEP for Bipolar Junction Transistors

The base-emitter voltage (V_{be}) has been found to be the most accurate and convenient TSEP for bipolar transistors [31]. This parameter has been accepted for temperature measurement primarily because its variation with temperature is almost constant when the collector current is held at a small, constant value [29]. Therefore, only a few points are necessary to generate a calibration curve which is valid over a wide range of temperatures.

5.3.2 TSEP Calibration

Calibration is performed to determine the relationship between junction temperature and the TSEP (V_{be}). This is accomplished by measuring the base-emitter voltage at various junction temperatures, while the collector current is held constant. Junction temperature is set by externally heating the transistor in an oven. A small collector current is used to ensure that the power dissipated in the device is negligible during calibration. Therefore, the junction temperature can be assumed to be equal to the oven temperature (providing that the transistor is allowed to stabilize after the oven temperature is changed). A typical calibration curve for the BLV93 transistor is shown in Figure 5.1. This plot shows the expected linear relationship between V_{be} and junction temperature, with a slope of -1.9 mV/°C.

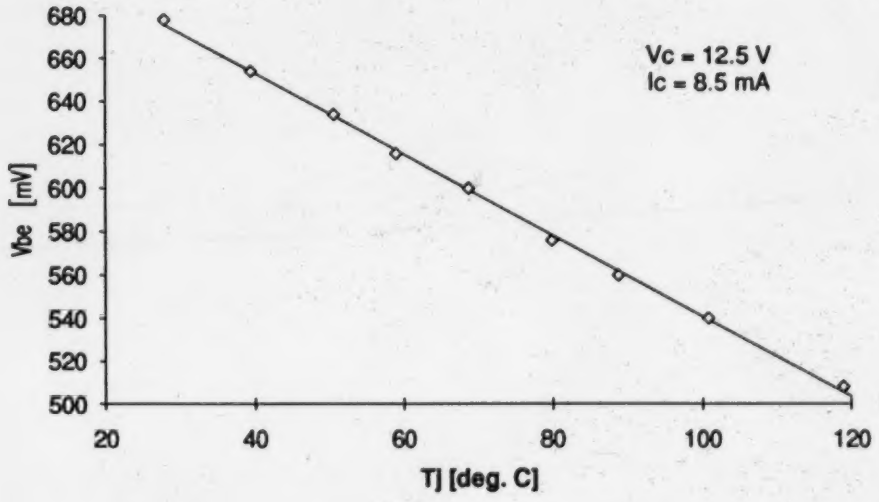


Figure 5.1 BLV93 V_{be} Calibration Curve

5.3.3 Difficulties with the Electrical Method

The electrical temperature measurement process is shown graphically in Figure 5.2. Normal device operation is periodically interrupted (~1% duty cycle) and the collector current is set to a small measuring value. This same collector current value is used in the generation of the calibration curve, as discussed above. After switching transients have subsided, the value of V_{be} representing the junction temperature is recorded. Finally, the measured value of V_{be} is translated to junction temperature using the previously generated calibration curve.

From the waveforms shown in Figure 5.2, it is apparent that there are some potential problems with the electrical method. First, cooling occurs in the device as soon as the heating current is removed. Therefore, V_{be} must be measured soon after switching to the measurement state to minimize errors due to cooling. These errors can be corrected by assuming a one-dimensional cooling model. This assumption is valid for the first 200 to 300 μs after the heating current is removed [31,32].

Measurement errors also result from transients which occur when the device is switched from the heating to the measuring state. To avoid these errors, the measurement of V_{be} must be delayed for several microseconds after the removal of the heating current.

Minimization of the two primary error sources cannot occur simultaneously, since one requires a short delay and the other a long delay. The optimum solution is obtained by considering the relative magnitudes of the errors, and the methods which are available to correct them. Errors due to cooling are relatively small, and can be corrected if the delay time is limited to about 200 μs. Transient errors are often large, and should be avoided since

they cannot be corrected. Therefore, accurate results are best obtained by using a relatively long delay time between the removal of the heating current and the measurement of V_{be}. If necessary, a correction algorithm based on one-dimensional cooling theory can be applied to extrapolate the zero-delay junction temperature.

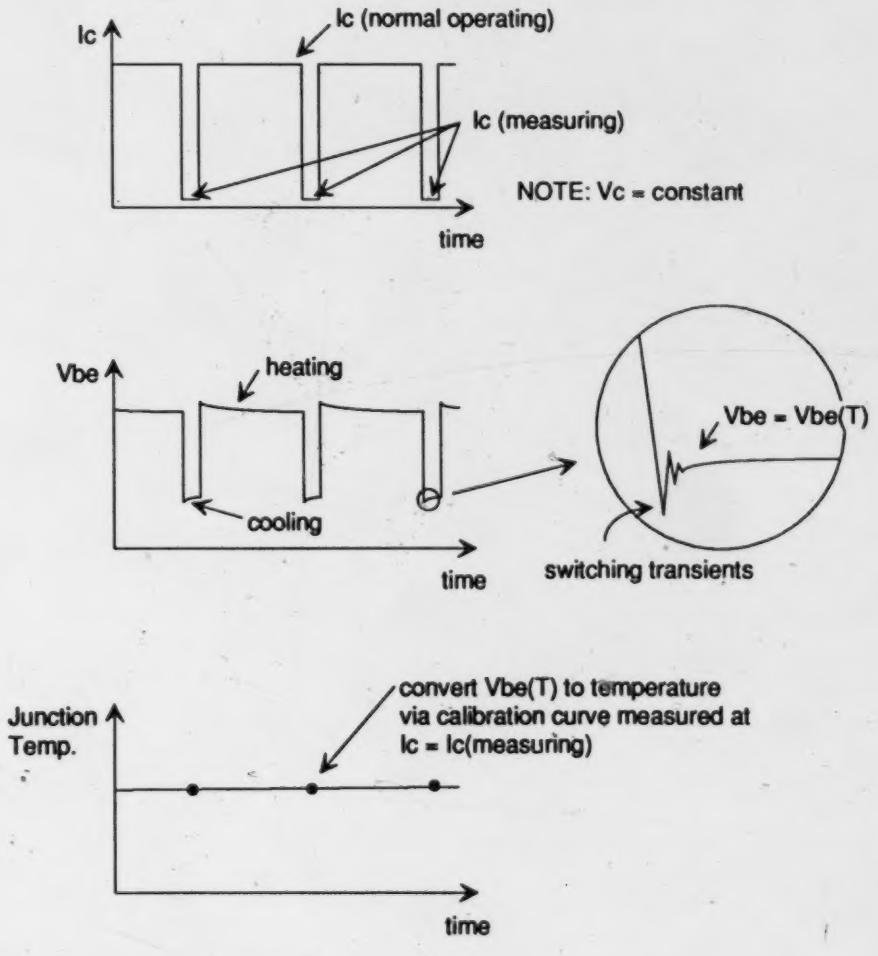


Figure 5.2. Electrical Temperature Measurement for a Bipolar Transistor

5.4 Electrical Temperature Measurement for RF Transistors

In the previous discussion of electrical junction temperature measurement, transistor self-heating is assumed to result from internally dissipated DC power. However, junction temperature data is required for a transistor operating in a class B amplifier configuration and dissipating RF power.

Self-heating is a low-frequency phenomenon which is primarily due to the DC component of dissipated power in the transistor. The period of a single RF cycle is approximately three orders of magnitude less than the device's thermal time constant. Therefore, it can be assumed that a negligible amount heating or cooling occurs during an RF cycle. This observation suggests that an equivalent DC operating condition can be used to determine the junction temperature of a transistor dissipating RF power.

However, the determination of this equivalent DC operating condition is complicated by several factors. The transistor's power density distribution is significantly different for the DC and RF modes of operation. Since the effective thermal resistance depends on this distribution, it is difficult to establish a relationship between the DC and RF cases. Assuming an equivalent DC operating condition exists, it cannot be derived using theoretical voltage and current waveforms. These do not include non-ideal saturation and parasitic effects, and measured waveforms do not represent the operation of the actual transistor chip. Therefore, it is unlikely that measurements made on a device dissipating DC power contain useful information that can be applied to the RF case.

Simplification of the RF temperature measurement problem is not possible. Thus, the standard electrical technique was enhanced to enable the

measurement of junction temperature for a transistor operating in a class B amplifier. The method and the accompanying control circuits are described in the following sections.

5.5 Experimental RF Temperature Measurement System

The concept of electrical junction temperature measurement is relatively simple; however, conflicting requirements complicate the design of a measurement circuit. A circuit is required which provides fast switching between the heating and measurement states, with minimal ringing (see Section 5.3.3). As well, the circuit must be compatible with a class B, RF power amplifier, which provides the desired RF dissipated power in the device.

The experimental system for measuring the temperature of a transistor operating in a class B amplifier is shown in Figure 5.3. Switching between the heating and measuring states is achieved in two steps:

1. The RF power (heating power) is removed,
2. The collector current is set to the small value used during the calibration of V_{be}.

The switching operation is provided by driving the amplifier with a series of RF pulses. The output from an 850 MHz power oscillator is switched by an intermediate amplifier and a function generator. The 100 Hz, 97.5% duty cycle RF pulse train provides a nearly continuous wave input to the class B amplifier. This ensures that the measuring pulses have a negligible effect on the steady-state temperature characteristics of the transistor.

A bias control circuit was designed to supply the constant measuring current when the amplifier is inactive. This circuit does not affect the normal operation of the class B amplifier.

5.5.1 Control Circuit Operation

The bias control circuit for the experimental temperature measurement system is shown in Figure 5.4. This circuit is designed to provide class B bias voltages during normal amplifier operation. When the amplifier is inactive, the circuit provides the necessary biasing to supply a small measuring current.

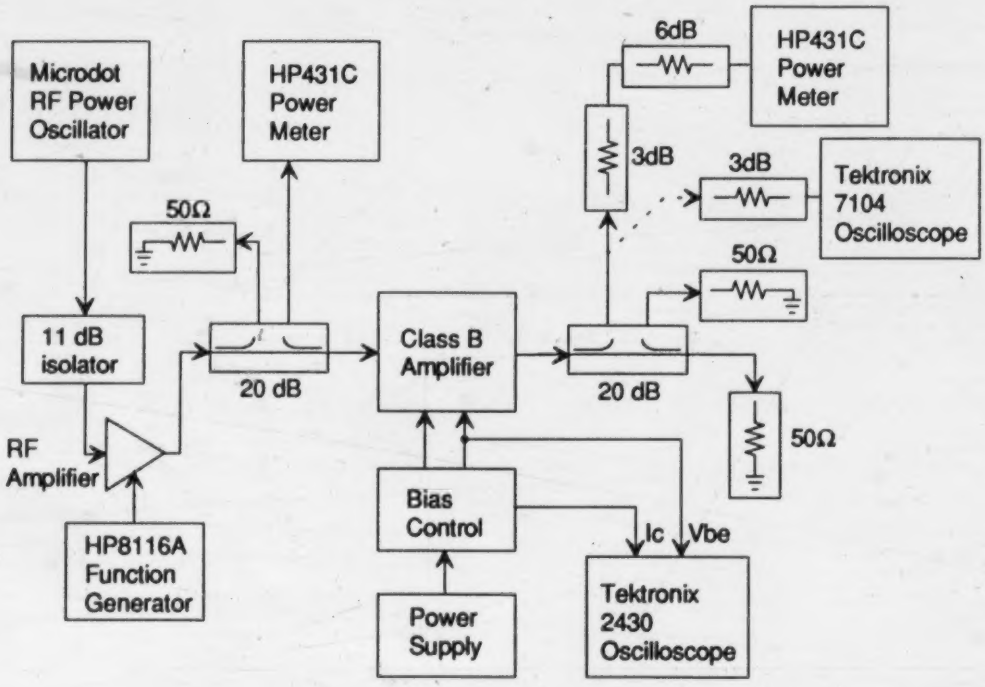


Figure 5.3 Experimental Setup for Electrical Temperature Measurement

The transistor is self-biased in the class B amplifier configuration, and therefore, it does not conduct in the absence of input RF power. Under this condition, the temperature measurement circuit is activated to supply a constant collector current. Amplifier A1 and the surrounding network (R1, R2, R3, and D1) provide a voltage of (V_{cc} - 20 mV) to the input of amplifier A2. Zener diode D1 ensures that this reference voltage is not susceptible to power

supply noise. The feedback circuit provides the necessary base current to hold the collector voltage at this same reference potential.

The voltage drop across R6 causes a constant measuring current of 8.5 mA to flow in the collector of the RF transistor (measured, including amplifier offset effects). The small value for I_C ensures a maximum temperature error of less than 1°C due to self-heating (estimated using the maximum thermal resistance value for the BLV93). High input impedance feedback and difference amplifiers are used to ensure that their input currents are negligible.

A difference amplifier, A3, is provided to monitor the collector current during switching from the heating to the measuring state. This enables the collector current to be checked before measuring the base-emitter voltage, to ensure that it is stable. Since the collector current is derived from the voltage drop across resistor R6, it must have a high power rating and low temperature coefficient to ensure that its value is constant for both the heating and measurement states.

During normal amplifier operation, a non-zero DC collector current is drawn through R6 (DC input power). This causes amplifier A2 to saturate in the negative direction, where it is unable to forward-bias the transistor. A bias adjustment network (D2, R8) is required to set the DC base voltage to zero, and maintain normal class B operation. The performance of the amplifier is monitored to ensure that the operation is as previously measured.

The power supply voltage is set so that the DC collector voltage is 12.5 V. The power supply voltage must be adjusted for each RF power level to maintain a constant DC collector voltage.

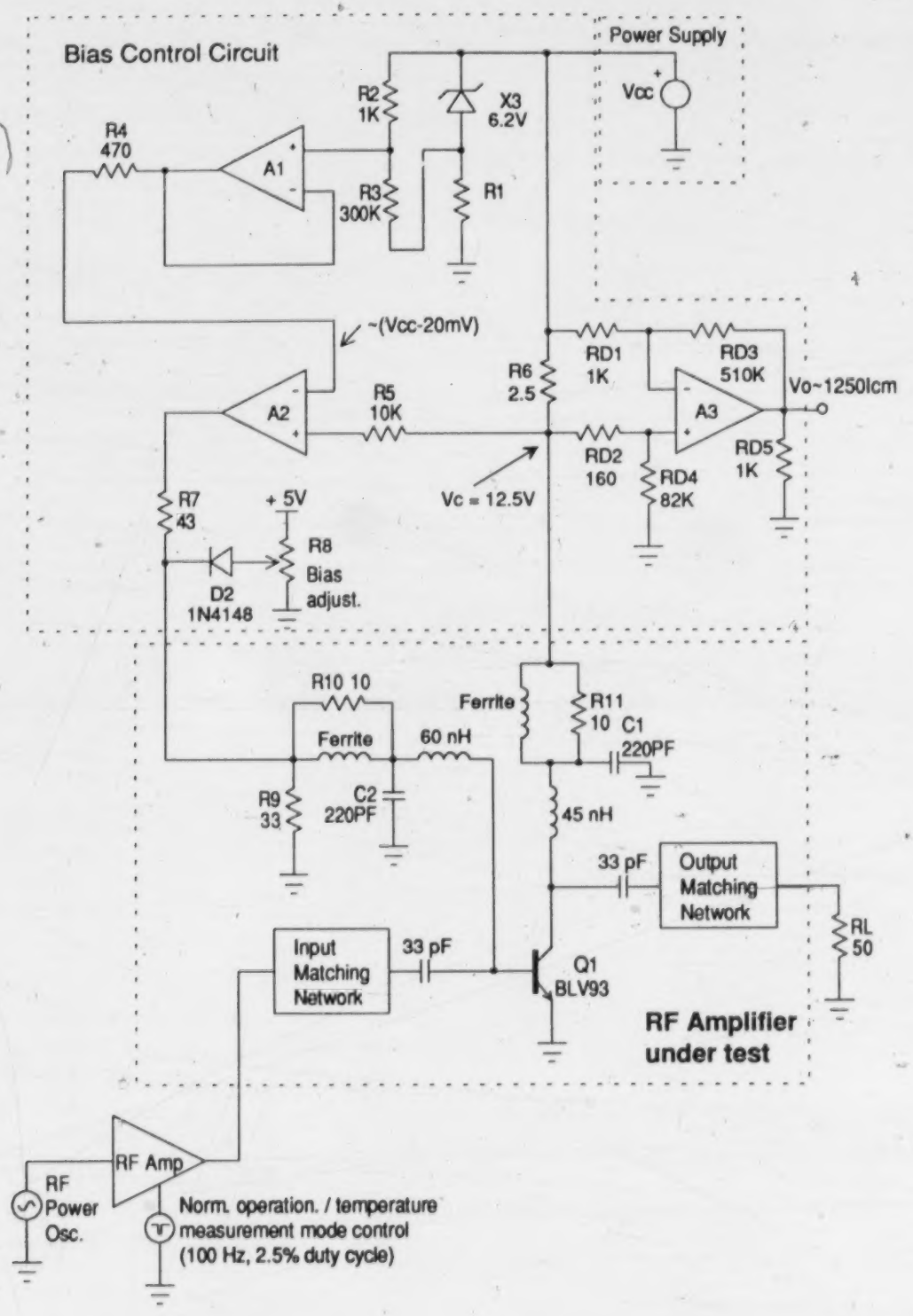


Figure 5.4 Control Circuit for Electrical Temperature Measurement

5.5.2 Results

The bias control circuit provides stable operation and fast switching from normal class B operation to the measuring state. Transients were observed to subside within 30 μs of switching for all operating conditions. The base-emitter voltage is measured at 50 μs and 250 μs after switching to determine the effect of cooling on the results. Measured junction temperature data are shown in Figure 5.5 for the BLV93 transistor operating in the experimental class B amplifier.

Measurements obtained with a 250 μs delay differ by only 2.2 to 4.3 °C from those obtained with the 50 μs delay. The difference between the measurements increases with the dissipated power level, which is consistent with a one-dimensional cooling model. This cooling model was not characterized, since the cooling errors are not significant enough to warrant the inclusion of correction techniques. Also, since the transients subside within 30 μs, the delay time can be reduced to increase the measurement accuracy, if desired.

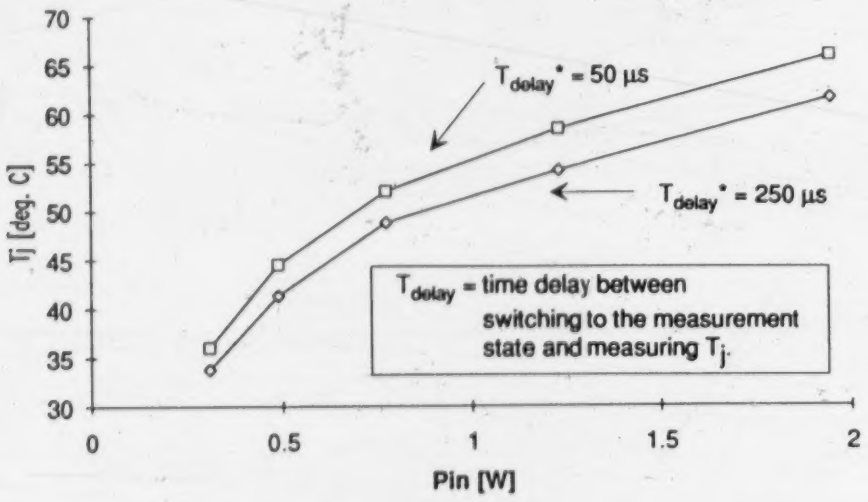


Figure 5.5 Measured Temperature Results

5.5.3 Transient Temperature Measurements

The method described above was developed to measure the steady-state junction temperature of a transistor operating in a class B amplifier. This technique can also be used to determine the transient thermal response of a transistor operating in a digital system.

The amplifier was used to amplify a train of RF transmit pulses, as in the proposed TDMA digital cellular network format [4]. The transmit frame time is of the same order as the device's thermal time constant, so the transistor temperature varies during the transmit frame time. The transient thermal response was determined by taking several junction temperature measurements at different times during the transmit pulse. The results of these measurements can be combined to provide an indication of the junction temperature variation versus time, as shown in Figure 5.6.

Although this project is concerned with steady-state amplifier simulation, a separate set of experiments was performed to confirm the validity of the proposed transient temperature measurement technique. The experimental transient temperature results are shown in Figure 5.7, when the amplifier is driven by a 50 Hz, 33% duty cycle RF pulse train (the signal specification for the digital cellular network [4]).

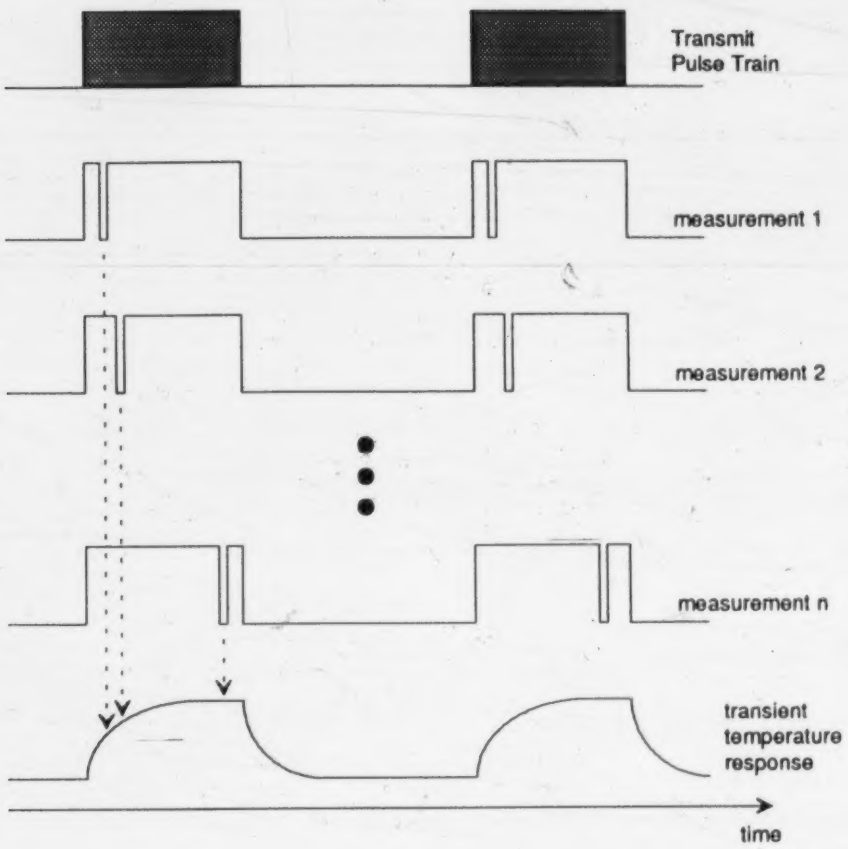


Figure 5.6 Measurement of Transient Thermal Behavior

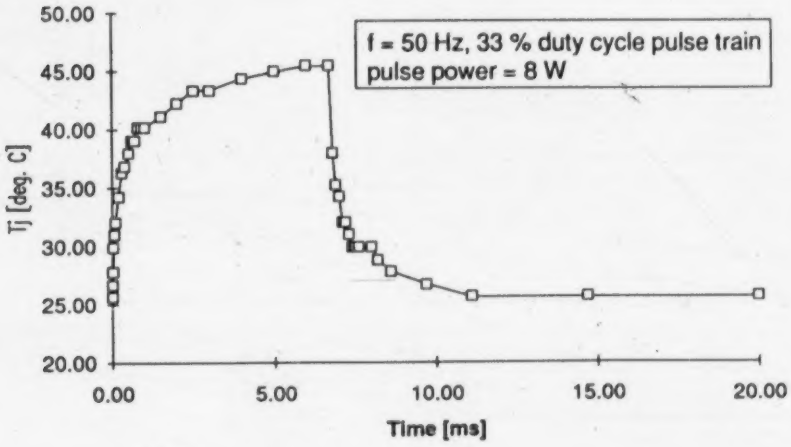


Figure 5.7 Transient Temperature Measurement Results

6. RF POWER AMPLIFIER SIMULATION

This chapter presents measured and simulated results which indicate the performance of the experimental class B amplifier. The previously determined RF power transistor and amplifier circuit models are combined to form a composite model for the class B amplifier. The complete non-linear amplifier model is used in a time-domain PSpice simulation, and the results are compared with the measured performance of the experimental amplifier. Measured junction temperature data are also included in the simulation to determine the temperature sensitivity of the model.

The results of the initial simulation runs are used to determine improvements for the RF transistor model. An upgraded transistor model is developed, and the resulting amplifier performance is presented. The effect of including junction temperature data is also investigated for the upgraded amplifier model.

6.1 Complete Amplifier Model

The complete amplifier model combines the models for the BLV93 RF power transistor and the class B matching circuits, as shown in Figure 6.1. All circuit element and model parameter values are determined using the previously described characterization procedures (see Chapters 3 and 4).

6.2 Simulation Procedure

The model presented above is used in a PSpice time-domain simulation to determine the steady-state amplifier performance. The use of the transient

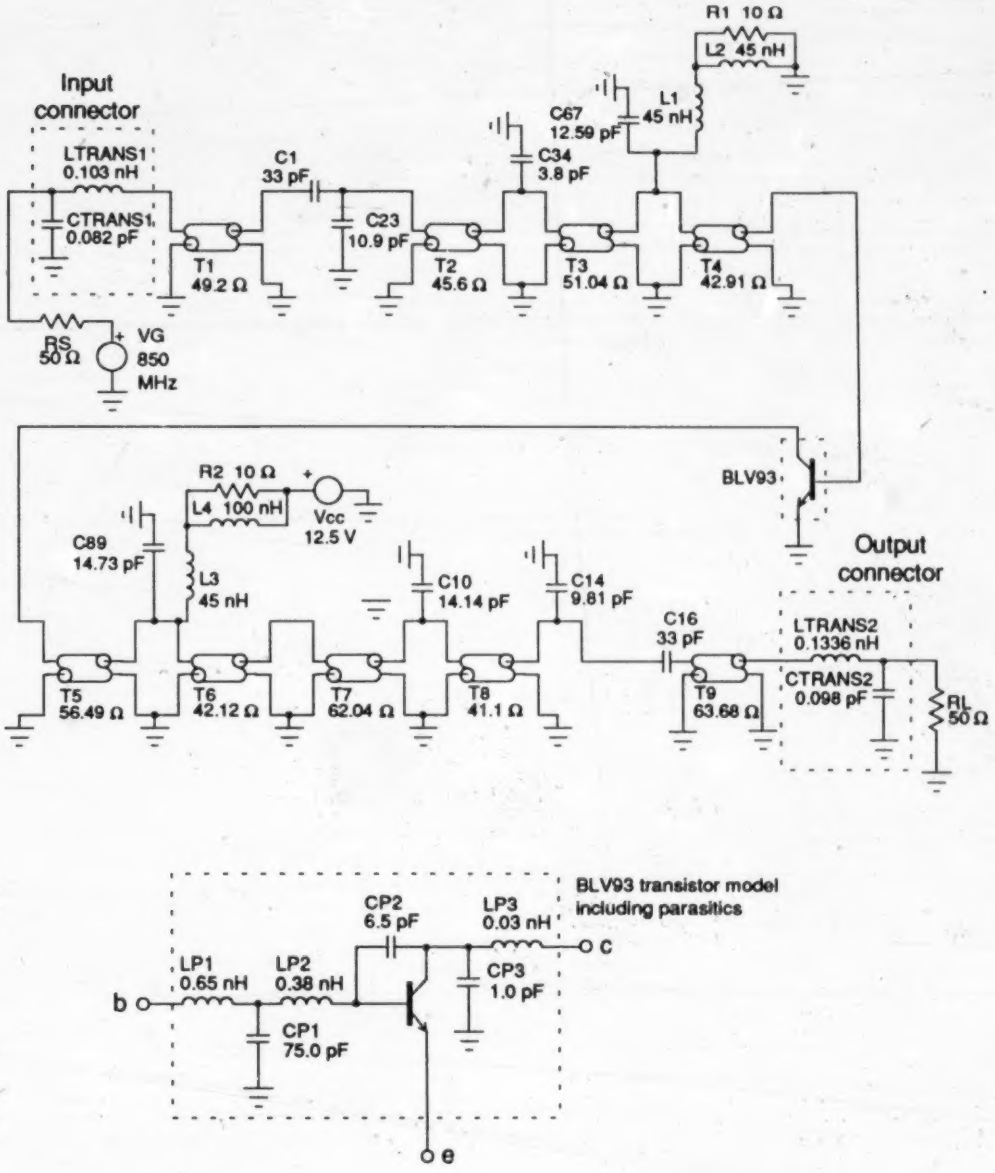


Figure 6.1 Complete Class B Amplifier Model

analysis mode is required in order to include the effects of various device non-linearities. A complete model of this type is necessary for communications applications, in order to determine the amplifier's gain and non-linear distortion

characteristics as a function of input power. These data cannot be accurately determined using a frequency-domain analysis.

6.2.1 Performance Indices

The performance of the amplifier model is determined by comparing the calculated RF output power and DC collector current (DC input power) with the corresponding experimental values. These performance indices are compared over an RF input power range of 25 dBm to 33 dBm. The lower input power limit represents the minimum value (measured) at which the self-biased amplifier is able to provide gain. Since in the class B configuration the transistor is not biased in the active region, a minimum value of RF input power is required for the transistor to conduct. The amplifier acts as an attenuator when the input power is below this value. The upper limit corresponds to the measured value of RF input power which enables the amplifier to supply its rated RF output power of 39 dBm (8 Watts).

Voltage and current waveforms are not used for comparison purposes since their measurement is difficult at high frequencies. Also, the introduction of RF probes alters the normal operation of the amplifier. Therefore, meaningful simulation results can only be obtained by providing additional model elements to represent the RF probes. Further additions to the amplifier are very undesirable, as they complicate the interpretation of the simulation results and make isolation of the model's error sources difficult. Therefore, it is less likely that discrepancies between the modeled and measured amplifier performance can be attributed to specific deficiencies in the transistor model.

6.2.2 Determination of Steady-State Performance

Initial simulation runs indicated that approximately 200 RF cycles were required for the 850 MHz amplifier response to stabilize, depending on the operating conditions. The variable time required to reach steady-state operation is a result of variable transistor impedances and feedback characteristics, which are non-linear functions of the operating conditions. All simulation results were obtained using a delay of 340 RF cycles (400 ns) to ensure consistent results. A separate simulation run was required to determine the amplifier performance for each value of RF input power.

6.3 Initial Amplifier Simulation

The initial amplifier model used the previously determined model parameter and element values (see Chapters 3 and 4). In this model, all Gummel-Poon model parameters and matching network element values are treated as fixed, known quantities. The transistor's parasitic network elements are only estimated by the characterization process (see Section 3.3.5.1). Therefore, these element values were manually adjusted (using the previously determined range of values) to minimize the deviation between the measured and modeled results at various RF input power levels. Several simulation runs were required to ensure that near-optimal performance is achieved, since the interaction of the input and output elements is complex.

The final parasitic network is able to match the amplifier input to the RF source ($P_{in} = P_{source}/2$) over the full RF input power range. However, a combination of element values which provide accurate modeling of the gain and efficiency over the same input power range could not be determined.

Feedback and output elements can be adjusted to provide satisfactory agreement for any single point on the measured output power curve, but not over the full range of input power. Parasitic element values were selected which provide the desired gain near the rated output power level. These values are indicated in Figure 6.1.

6.3.1 Results Neglecting Junction Temperature

The results of the time-domain simulations are shown in Figures 6.2 and 6.3. The simulated RF output power is within 0.6 dB of the measured power near the rated value of 39 dBm (8 W). However, the model is less accurate when the input power is reduced, differing by 4 dB for an input power of 26 dBm. DC collector current is not modeled very accurately, as it is consistently underestimated by about 100 mA.

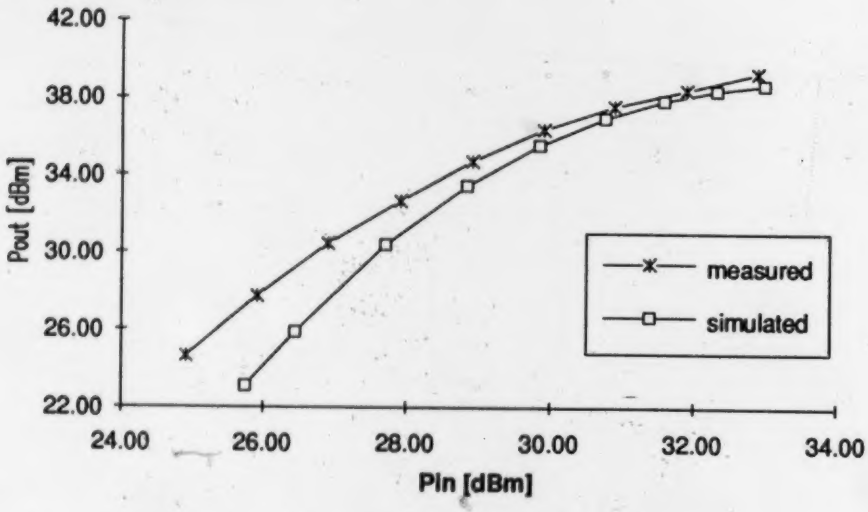


Figure 6.2 Pout versus Pin (neglecting Tj)

In analyzing the above results, it is apparent that the simulated amplifier operates as a saturating class C amplifier rather than a class B amplifier. This is indicated by the following observations:

1. The simulated amplifier efficiency is consistently higher than the experimental amplifier (not explicitly shown in the curves).
2. The output power falls quickly as the input power is reduced.
3. The simulated amplifier response starts to saturate in the high power region.

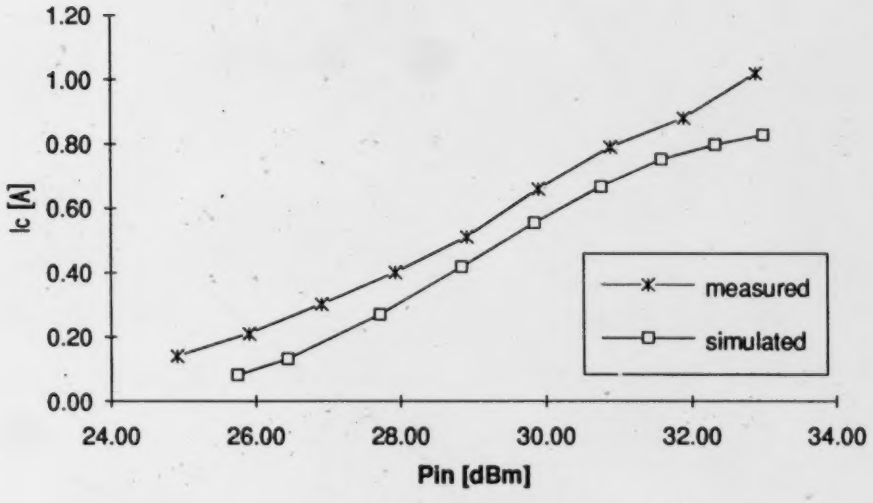


Figure 6.3 $I_{C(DC)}$ versus Pin (neglecting Tj)

A class C amplifier is more efficient than an equivalent class B amplifier. This increased efficiency is a result of a reduced conduction angle, and is achieved by applying a negative bias voltage to the base of the transistor. The reduced conduction angle for the class C amplifier necessitates a higher peak collector current as compared to a class B amplifier, to supply the same amount of output power. As discussed earlier, self-biased amplifiers require a minimum input power level before they can provide amplification. The negatively-biased base and increased peak current requirement cause this minimum input power level to be higher for a class C amplifier than for a class B amplifier. This is consistent with the results of Figure 6.2, where a minimal input power of 30 dB

is necessary before significant gain is obtained. The error sources which cause this incorrect amplifier operation are discussed in Section 6.4.1.

The output power and DC collector current curves also indicate that the simulated amplifier begins to saturate at high power levels (both curves start to level off). Additional simulation runs using input powers in the 34 dBm to 36 dBm range confirmed this behavior (these results are not shown on the graphs).

The results also indicate that junction temperature effects may not be responsible for the inaccuracy of the model. The maximum performance deviations are observed at the low power range, where minimal self-heating is experienced. This is partially a result of the selected parasitic network values, which were optimized to provide the desired gain near the rated output level. Therefore, junction temperature effects are investigated in the following section, prior to making adjustments to the transistor model.

6.3.2 Effect of Including Junction Temperature

The temperature sensitivity of the model is determined by including measured junction temperature data in the simulation. No other changes are made to the transistor or amplifier models (temperature-dependent transistor model parameters are calculated internally by PSpice). The results are shown in Figures 6.4 and 6.5.

The results are virtually identical to the previous simulation results (obtained for a constant $T_j = 27$ °C). These results were unexpected since several of the Gummel-Poon model parameters are strong functions of temperature (see Section 3.2.2).

The above results were confirmed by additional simulation runs which included exaggerated junction temperature data ($\Delta T = T_{(measured)} - 27$ °C, was

multiplied by a factor of 2). An analysis of the results indicates that although the active device characteristics change significantly with temperature, the overall transistor performance is largely determined by the package parasitics.

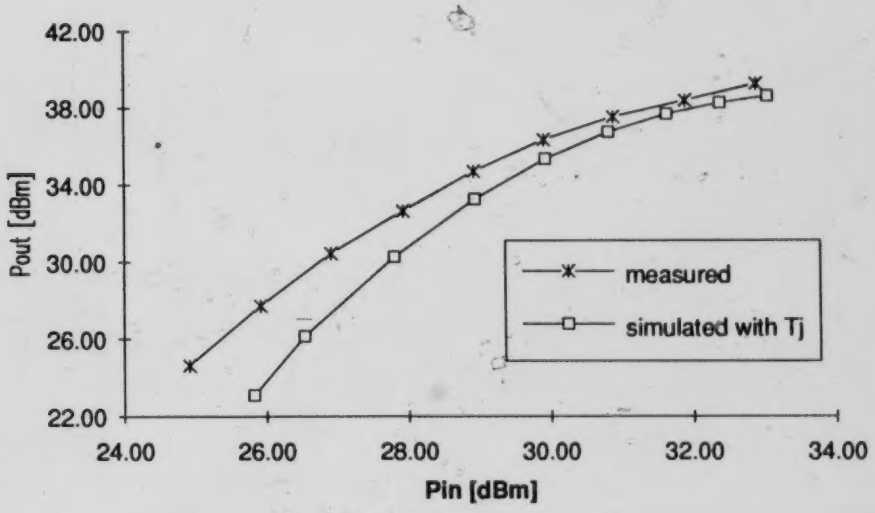


Figure 6.4 Pout versus Pin (including Tj)

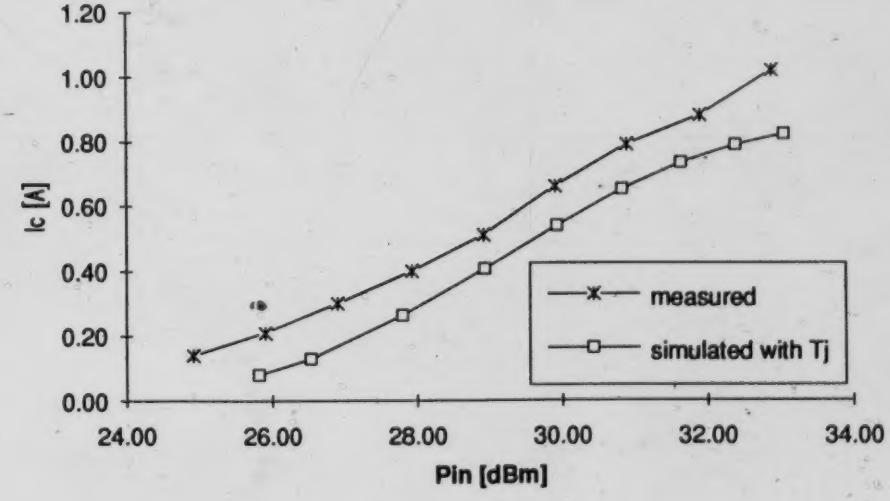


Figure 6.5 $I_{C(DC)}$ versus Pin (including Tj)

The transistor's input impedance is predominantly determined by the input parasitic network. This is seen in the nearly identical base voltage waveforms in Figure 6.6, calculated at 27 °C and 66 °C. Although the transistor's input diode current is a strong function of temperature, it represents a maximum of 5% of the total input base current (for the majority of the RF cycle, this current component represents less than 1% of the total base current).

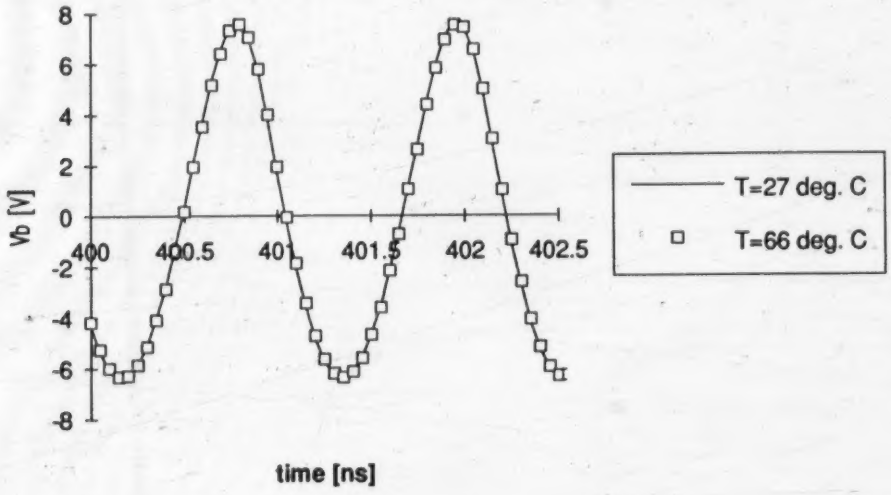


Figure 6.6 Base Voltage Waveform

Amplifier gain was also expected to vary significantly with junction temperature. Simulation of an ideal class B amplifier indicates that the gain can change by as much as 3 dB when the temperature is increased from 27 °C to 66 °C. This temperature-dependent gain is stabilized in the real amplifier by large base-collector feedback elements. This is indicated in Figure 6.7, where the output voltage waveforms are virtually independent of junction temperature. (The non-ideal collector waveforms are a result of harmonic generation and saturation effects. Their shapes are consistent with previous modeling results

[12,33].) Figure 6.8 indicates that the internal base-emitter voltage is automatically reduced by the parasitic feedback network to maintain a constant output power. The feedback provided by the emitter ballast resistors also assists in stabilizing the RF gain. However, this feedback component is very small compared to that provided by the base-collector capacitance. The primary function of these resistors is to ensure a relatively uniform current (and temperature) distribution throughout the transistor. The above conclusions are also supported by base and collector current waveforms (not shown).

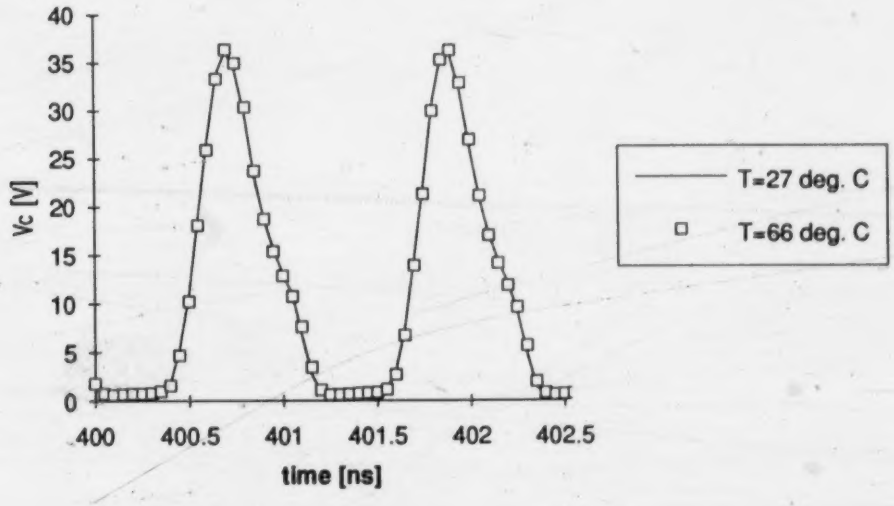


Figure 6.7 Collector Voltage Waveform

6.4 Amplifier Simulation Using an Improved Transistor Model

Preliminary simulation results indicate that the simulated amplifier behaves as a saturating class C amplifier. This section outlines the improvements which were made to correct the transistor model inaccuracies, and presents the ensuing simulation results for the class B amplifier.

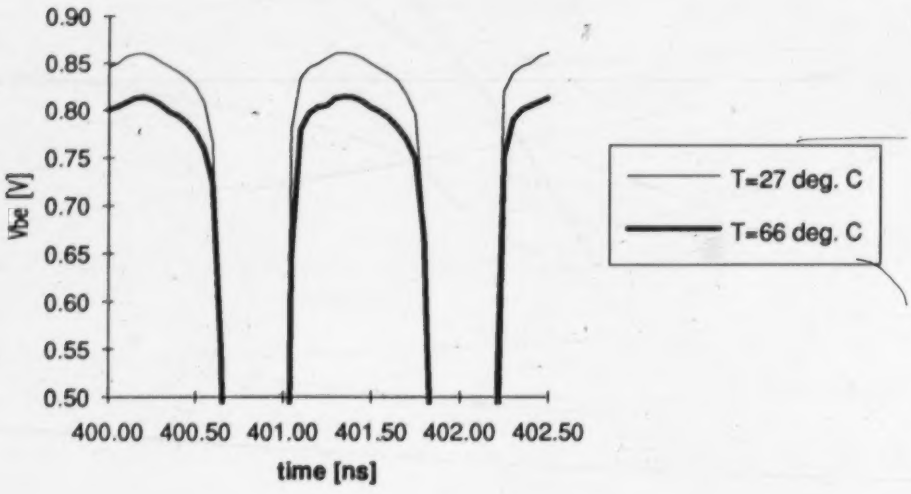


Figure 6.8 Base-Emitter Junction Voltage Waveform

6.4.1 Transistor Model Improvements

The class C configuration is differentiated from the class B configuration by the negative DC bias voltage at the transistor's base terminal. This reduces the conduction angle and leads to increased amplifier efficiency. Although a negative base voltage is not provided explicitly in the model, the DC component of the base current can cause this effect if it flows through a sufficiently large base resistor. The resulting DC voltage drop causes a negative voltage at the internal base node, since the base lead is connected to DC ground via an RF choke. Base resistance is known to be a difficult parameter to characterize accurately. The determined value is very sensitive to the measurement technique used in the extrapolation process [18]. Since there is no measurement technique available in which the transistor operates close to the large-signal class B condition, the extracted value is only an estimate of the actual base resistance value. Also, the single resistor represents a very simple model for the complex base resistance relationship (see Chapter 3).

The modeled amplifier was also observed to enter saturation in the high power region. This is primarily a result of the simple saturation model which is provided by the collector resistor, r_c. The nominal value determined in the extraction phase represents the upper limit for r_c. The lower saturation value was not determined, but should be considered for simulating the class B amplifier.

6.4.2 Final Simulation Results

Several simulation runs were performed to determine the optimal values of r_b and r_c (1.4Ω and 0.25Ω, respectively). The parasitic network elements were also readjusted, but this did not improve the simulation results. Therefore, these element values were kept at their previously determined values. The final results of the simulation with the improved transistor model are shown in Figures 6.9 and 6.10.

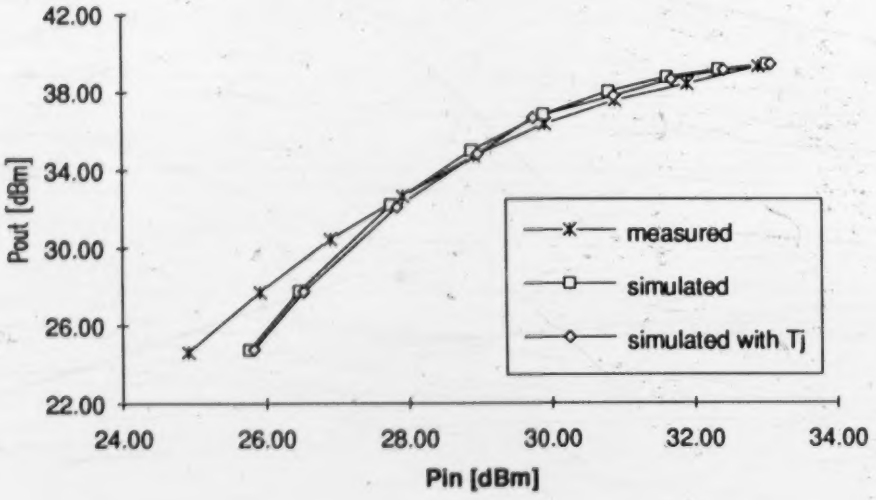


Figure 6.9 Pout versus Pin (improved transistor model)

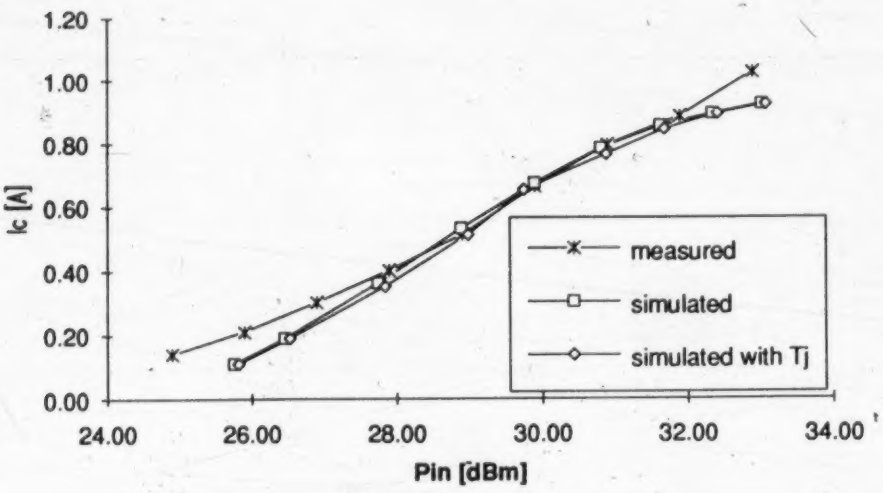


Figure 6.10 $I_{C(DC)}$ versus Pin (improved transistor model)

The simulated gain and collector current are significantly improved using the improved transistor model. The simulated RF output power is observed to be within 0.5 dB of measured near the rated value of 39 dBm, and within 2.2 dB for an input power of 26 dBm. The model maintains the 0.5 dB accuracy (approximately) for RF gain over a 5 dB range of RF input power. This is essentially the usable operating range of the amplifier, since when Pin is less than 27 dBm, the actual amplifier gain is 3 dB lower than its maximum value (a significant amount when the maximum gain is only 6.6 dB).

The deviation at the low power region underlines the fact that the parasitic network model is a simplified representation of the actual device parasitics, and is only valid over a limited operating range. The inaccuracies in the transistor model combined with those of the matching circuit models, tend to alter the conduction angle of the amplifier. Therefore, the simulated amplifier gain decreases significantly after the input power is reduced below 28 dBm.

The simulation accuracy for the collector current is improved significantly over the majority of the input power range. As with the RF output power, simulated collector current accuracy is reduced when the input power is less than 28 dBm. This also supports the previous conclusion that the conduction angle of the simulated amplifier does not correspond to the experimental amplifier. Differences between the simulated and measured collector current data are also observed in the high power region, as the simulated amplifier is observed to enter saturation. Although the saturation model is improved by adjusting the collector resistance value, it is apparent that further improvement can only be achieved by including a more comprehensive saturation model for the transistor.

As in the previous simulation runs, the inclusion of junction temperature has virtually no effect on the accuracy of the results. Although the base resistor value has been reduced in the improved transistor model, the device's input impedance is still dominated by the package parasitics. The large base-collector feedback component also regulates the RF gain characteristic with respect to junction temperature.

The good agreement obtained between the measured and modeled amplifier performance emphasizes the importance of the characterization procedures outlined in Chapters 3 and 4. Although the transistor has a complex internal structure consisting of multiple devices, a simplified model can be used to provide a manageable and accurate amplifier model, if it is characterized correctly. This is particularly important so that transistor models can be characterized using data measured at the device terminals (on the composite device). While it is desirable to develop a model which is accurate for all operating conditions, it is apparent that this is an unrealistic goal for an

RF device. This is also unnecessary, as shown in the final simulation results, since the amplifier was simulated accurately over most of its useful operating range.

7. SUMMARY AND CONCLUSION

The development of accurate transistor models is essential if simulation is to be used as a large-signal RF design tool. To date, transistor models do not provide the accuracy necessary for RF design. The models are able to describe the operation of the transistor only after fine-tuning the model parameters to match the predicted and measured RF output power and DC collector current responses. It is well known that transistors delivering relatively large amounts of RF power also experience self-heating due to internally dissipated power. This thesis has investigated the effect of using a temperature-dependent model for simulating an RF power transistor used in a class B amplifier as a function of RF input power.

Several transistor models and simulation techniques were investigated to determine the best modeling method for the RF power transistor. An equivalent circuit model and a time-domain simulation were necessary to provide the accuracy required for an RF design tool. Specifically, the Gummel-Poon equivalent circuit model was shown to provide a comprehensive model for first and second-order effects, which enabled the modeling of both linear and non-linear transistor behavior. Package parasitics were also included by adding passive elements to the transistor circuit model. All model parameters were determined from terminal measurements made on normal, packaged devices.

The RF power transistor has a complex internal structure containing multiple devices using an interdigitated design. The DC performance of the composite device was consistent with a single, large-area transistor. Similarly, the low-frequency AC performance was adequately represented by a single transistor model. Standard extraction techniques provided model parameter

values which accurately described the device behavior over a wide DC collector current range (100 μA to 1 A). The temperature dependence of several DC model parameters was also consistent with previously developed relationships.

RF device characterization was very difficult as the operation of the device was significantly different at RF than at DC. Therefore, various model parameters determined from DC measurements were invalid at RF. Specifically, the base and collector resistance values did not accurately describe the RF input impedance and transistor saturation behavior, respectively. Large-signal RF measurement techniques could not be used since the non-linear active device characteristics are masked by the effects of package parasitics, when measured at the transistor terminals. Transistor chip data could not be de-embedded from the terminal data without an accurate description of the equivalent parasitic network.

The development of an accurate package parasitic model was the most difficult part of the RF transistor model development process. Simplification of the complex device structure was necessary to provide a manageable and computationally efficient model. However, it was these simplifications which limited the model's accuracy and usefulness as a design tool. Measurement techniques were not available to determine the transistor performance at various physical locations within the device, to enable the development of a complex, multi-device model. A general parasitic network topology was assumed which used lumped circuit elements. This network represented a very simple description of the actual device structure. The nature of the distributed parasitics effects were unknown, so that transmission line models could not be specified to describe them accurately. A pseudo-distributed model was provided for the base-emitter matching network which consisted of a multi-section LC network.

An optimization technique was used to characterize the parasitic network and to investigate the performance of various network topologies. Models of various complexity were used, but none was able to compensate for the simplifications made by neglecting the multi-device aspects of the transistor. Inaccuracies in the intrinsic transistor model and the finite capabilities of the optimizer also prevented the determination of a unique set of network element values. The procedure provided a range of values which could be used in fine-tuning the model for simulation of the power amplifier. These results were useful, but did not enable the prediction of the amplifier's output power and DC collector current performance prior to its construction.

The performance of the transistor model was determined using experimental data obtained using a class B power amplifier. The merits of the optimization technique were demonstrated by the accurate characterization of the amplifier input and output matching circuits. For these cases, the circuit topologies were known, and the optimizer was only required to perform fine-tuning. Also, distributed transmission line models were used since the nominal values of all parameters were known.

The initial performance of the model was unsatisfactory, primarily due to the inadequate parasitic network element values and inaccurate base and collector resistor values. The model was able to provide good agreement between the measured and modeled performance after adjusting these parameters.

Although the active device characteristics were observed to change significantly with junction temperature, the performance of the RF transistor model was largely determined by the package parasitics. The use of temperature-dependent model parameters and junction temperature data did not significantly improve simulation accuracy, and therefore, the temperature

behavior of the transistor chip had a secondary role in the overall performance of the transistor. The complex parasitic network provided a feedback network which regulated the RF gain and efficiency relative to junction temperature.

These results enable the initial design of RF amplifiers to be performed without considering junction temperature, provided that the maximum specified junction temperature is not exceeded. As well, it is possible to make integrated amplifiers (MMICs) insensitive to temperature by surrounding the active device by a suitable passive network (similar to the parasitic network of the BLV93 RF power transistor). Sensing diodes and feedback circuits are not necessary for thermal stabilization of class B amplifiers.

As a consequence of the work performed in this project, the following topics have been identified for future research:

1. Development of a base resistance model which is accurate for both small and large values of base current. Non-linear elements may be necessary to accurately describe current crowding effects. This model should be less sensitive to the extraction techniques than the one presented in this thesis.

2. Investigation of the model performance when a more comprehensive saturation is included. This model should also be less sensitive to the extraction techniques used so that it can be characterized at DC or at low frequencies.

3. Investigation of alternative methods of characterizing complex parasitic effects, such as those found in a multi-transistor device. Ideally, these methods would use terminal measurements made on normal, packaged devices.

BIBLIOGRAPHY

[1] I.E. Getreu, *Modeling the Bipolar Transistor*, Elsevier Scientific Publishing Company, New York, 1976.

[2] J. Vidkjaer, "A Describing Function Approach to Bipolar RF-PowerAmplifier Simulation", *IEEE Transactions on Circuits and Systems*, Vol. CAS-28, No. 8, August 1981, pp. 758-767.

[3] W. Banzhaf, *Computer-aided Circuit Analysis Using SPICE*, Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1989, pp. 5-7.

[4] EIA/TIA Interim Standard, *Cellular System Dual-Mode Mobile Station - Base Station Compatibility Standard*, IS-54, Electronic Industries Association, May 1990, pp. 8-15.

[5] V. Rizzoli, A. Neri, "State of the Art and Present Trends in Nonlinear Microwave CAD Techniques", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 36, No. 2, February 1988, pp. 343-365.

[6] V. Rizzoli, A. Lipparini, F. Mastri, "Computation of Large-signal S-parameters by Harmonic-Balance Techniques", *Electronics Letters*, Vol. 24, No. 6, March 17, 1988, pp.329-330.

[7] P.D. van der Puije, S.R. Mazumder, "Two-signal Method of Measuring the Large-signal S-parameters of Transistors", *IEEE Microwave Symposium*, 1978, pp. 263-266.

[8] W.H. Leighton, R.J. Chaffin, J.G. Webb, "RF Amplifier Design with Large-Signal S-Parameters", *IEEE Transactions on Microwave Theory and Techniques*, December 1973, pp. 809-814.

[9] O. Pitsalis Jr., R.A. Gilson, "Broad-Band Microwave Class-C Transistor Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-21, No. 11, November 1973, pp. 660-668.

[10] K.S. Kundert, G.B. Sorkin, A. Sangiovanni-Vincentelli, "Applying Harmonic Balance to Almost-Periodic Circuits", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 36, No. 2, February 1988, pp. 366-378.

[11] D.O. Pederson, "A Historical Review of Circuit Simulation", *IEEE Transactions on Circuits and Systems*, Vol. CAS-31, No. 1, January 1984, pp. 103-111.

[12] J. Vidkjaer, "A Computerized Study of the Class-C-Biased RF-Power Amplifier", *IEEE Journal of Solid-State Circuits*, Vol. SC-13, No. 2, April 1978, pp. 247-258.

[13] J. Lange, "A Survey of the Present State of Microwave Transistor Modeling and Simulation as Applied to Circuit Design", *IEEE Transactions on Electron Devices*, Vol. ED-18, No. 12, December 1971, pp. 1168-1174.

[14] R.G. Harrison, "Computer Simulation of a Microwave Power Transistor", *IEEE Journal of Solid-State Circuits*, Vol. SC-6, No. 4, August 1971, pp. 226-235.

[15] H.K. Gummel, H.C. Poon, "An Integral Charge Control Model of Bipolar Transistors", *The Bell System Technical Journal*, May-June 1970, pp. 827-852.

[16] P.R. Gray, R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons Inc., Toronto, 1984, pp. 31-46.

[17] P.E. Gray, D. Dewitt, A.R. Boothroyd, J.F. Gibbons, *Physical Electronics and Circuit Models of Transistors*, John Wiley and Sons Inc., Toronto, 1964, pp. 121-145.

[18] P. Antognetti, G. Massobrio, *Semiconductor Device Modeling with SPICE*, McGraw-Hill Book Company, Toronto, 1988, pp. 101-103, 211-229.

[19] I.M. Gottlieb, *Solid-State High-Frequency Power*, Reston Publishing Company, Inc., Reston, 1982, pp. 57-58.

[20] J.C. Bowers, N. English, H.A. Nienhaus, "Parameter Determination Techniques for the Gummel-Poon CAD Transistor Model", *IEEE Power Electronics Specialists Conference '80 Record*, Atlanta, Georgia, 1980, pp. 83-90.

[21] L.J. Giocoletto, "Measurement of Emitter and Collector Series Resistances", *IEEE Transactions on Electron Devices*, Vol. ED-19, May 1972, pp. 692-693.

[22] W.C. Dillard, Jr., The Temperature Dependence of Hybrid-Pi Circuit Parameters, *Proceedings of the IEEE University/Government/Industry Microelectronics Symposium*, Auburn, Alabama, 1985, pp. 122-128.

[23] T.B. Mills, S-Parameters in SPICE, *RF Design*, June 1989, pp. 45-48.

[24] R.G. Gough, High-Frequency Transistor Modeling for Circuit Simulation, *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 4, August 1982, pp. 666-670.

[25] H.L. Krauss, C.W. Bostian, F.H. Raab, *Solid State Radio Engineering*, John Wiley and Sons Inc., Toronto, 1980, pp. 394-399.

[26] A.S Sedra, K.C. Smith, *Microelectronic Circuits, Second Ed.*, Holt, Rinehart and Winston, Toronto, 1987, 555-560.

[27] J. Lange, W.N. Carr, "An Application of Device Modeling to Microwave Power Transistors", *IEEE Journal of Solid-State Circuits*, Vol. SC-7, No. 1, February 1972, pp. 71-80.

[28] R.K. Gupta, "Intermodulation Distortion Analysis of a Microwave GaAs FET Amplifier", *PhD. Thesis*, University of Alberta, 1980, pp. 52-57.

[29] F.F. Oettinger, D.L. Blackburn, S. Rubin, Thermal Characterization of Power Transistors, *IEEE Transactions on Electron Devices*, Vol. ED-23, No. 8, August 1976, pp. 831-838.

[30] J.G.A. Scholten, *Thermal Aspects of Flange-mounted R.F. Power Transistors, Electronic Components and Applications*, Vol. 6, No. 2, 1984, pp. 96-106.

[31] D.L. Blackburn, A Review of Thermal Characterization of Power Transistors, *IEEE Semiconductor Thermal and Termperature Measurement Symposium*, 1988, pp. 1-7.

[32] D.L. Blackburn, F.F. Oettinger, Transient Thermal Response Measurements of Power Transistors, *IEEE Transactions on Industrial Electronics and Control Instrumentation*, Vol. IECI-22, No. 2, May 1975, pp. 134-141.

[33] R.L. Bailey, "Large-Signal Nonlinear Analysis of a High-Power High-Frequency Junction Transistor", *IEEE Transactions on Electron Devices*, Vol. ED-17, No. 2, February 1970, pp. 108-119.

APPENDIX A

Philips BLV93 U.H.F. Power Transistor

Data Sheet

U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in mobile radio transmitters in the 900 MHz communications band.

Features:

- multi-base structure and emitter-ballasting resistors for an optimum temperature profile
- internal input matching to achieve an optimum wideband capability and high power gain
- gold metallization ensures excellent reliability.

The transistor has a 6-lead flange envelope with a ceramic cap (SOT-171). All leads are isolated from the flange.

QUICK REFERENCE DATA

R.F. performance at T_h = 25 °C in a common-emitter class-B test circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	12,5	900	8	> 6,5	> 50
	9,6	900	6	typ. 6,0	typ. 59

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	I_C; $I_{C\,AV}$	max.	1,6 A
(peak value); f > 1 MHz	I_{CM}	max.	4,8 A
Total power dissipation			
at T_{mb} = 67 °C	$P_{tot(dc)}$	max.	18 W
at T_{mb} = 67 °C; f > 1 MHz	$P_{tot(rf)}$	max.	24 W
Storage temperature	T_{stg}		−65 to + 150 °C
Operating junction temperature	T_j	max.	200 °C

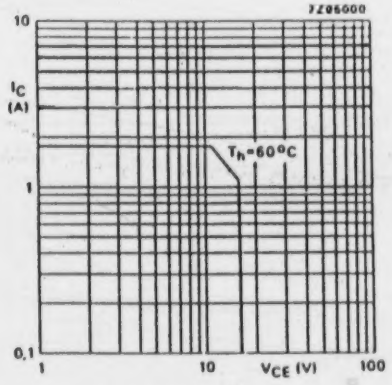


Fig. 2 D.C.-SOAR.

$R_{th\,mb\text{-}h}$ = 0,4 K/W

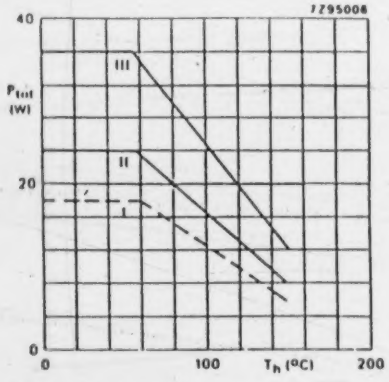


Fig. 3 Power/temperature derating curves.

1 Continuous operation
II Continuous operation (f > 1 MHz)
III Short-time operation during mismatch; (f > 1 MHz)

THERMAL RESISTANCE

Dissipation = 12 W; T_{mb} = 112 °C

From junction to mounting base			
(d.c. dissipation)	$R_{th\,j\text{-}mb(dc)}$	max.	7,0 K/W
(r.f. dissipation)	$R_{th\,j\text{-}mb\,(rf)}$	max.	5,2 K/W
From mounting base to heatsink	$R_{th\,mb\text{-}h}$	max.	0,4 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 20 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage open base; I_C = 40 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage open collector; I_E = 2 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	10 mA
Second breakdown energy L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	E_{SBR}	>	2 mJ
D.C. current gain I_C = 1,2 A; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz* $-I_E$ = 1,2 A; V_{CE} = 12,5 V	f_T	typ.	4 GHz
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	15 pF
Feed-back capacitance at f = 1 MHz I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	9 pF
Collector-flange capacitance	C_{cf}	typ.	2 pF

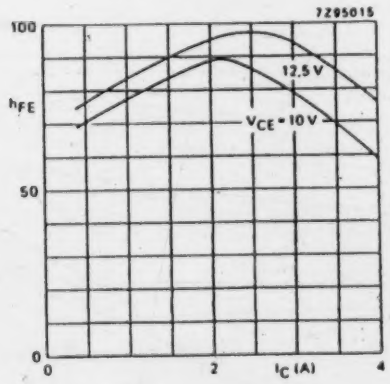


Fig. 4 T_j = 25 °C; typical values.

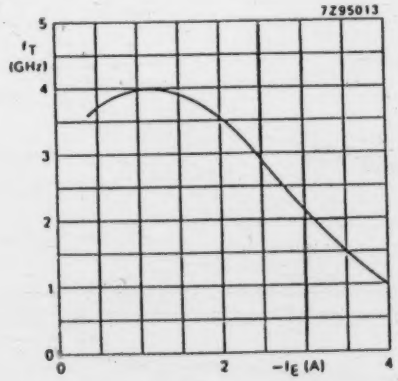


Fig. 5 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typical values.

* Measured under pulse conditions: t_p = 50 μs; δ < 1%.

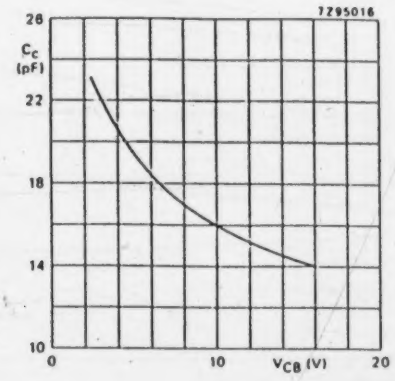


Fig. 6 $I_E = i_e = 0$; f = 1 MHz; typical values.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_h = 25 °C.

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C A	η_C %
narrow band; c.w.	12,5	8	< 1,8 typ. 1,5	> 6,5 typ. 7,3	< 1,28 typ. 1,1	> 50 typ. 58
	9,6	6	typ. 1,5	typ. 6,0	typ. 1,05	typ. 59

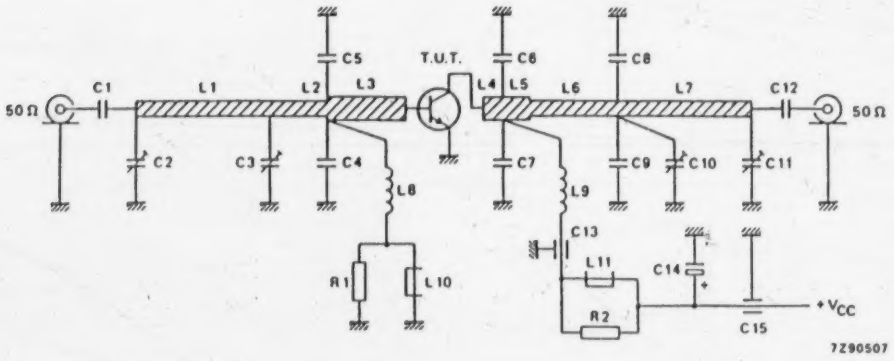


Fig. 7 Class-B test circuit at f = 900 MHz.

List of components:

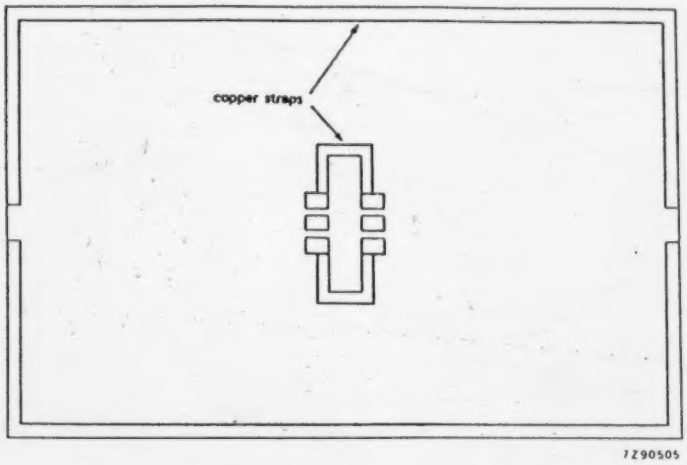
C1 = C12 = 33 pF multilayer ceramic chip capacitor
C2 = C3 = C10 = C11 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C4 = C5 = 4,7 pF multilayer ceramic chip capacitor*
C6 = C7 = 5,6 pF multilayer ceramic chip capacitor*
C8 = C9 = 3,3 pF multilayer ceramic chip capacitor*
C13 = 10 pF ceramic feed-through capacitor
C14 = 6,8 μF (63 V) electrolytic capacitor
C15 = 330 pF ceramic feed-through capacitor

L1 = L7 = 50 Ω stripline (29,0 x 2,4 mm)
L2 = 50 Ω stripline (6,0 mm x 2,4 mm)
L3 = 42,7 Ω stripline (13,1 mm x 3,0 mm)
L4 = 42,7 Ω stripline (4,4 mm x 3,0 mm)
L5 = 42,7 Ω stripline (4,6 mm x 3,0 mm)
L6 = 50 Ω stripline (11,0 x 2,4 mm)
L8 = 60 nH; 4 turns closely wound enamelled Cu-wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L9 = 45 nH; 4 turns enamelled Cu-wire (1,0 mm); length 6 mm; int. dia 4 mm; leads 2 x 5 mm
L10 = L11 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)

R1 = R2 = 10 Ω ± 10%; 0,25 W, metal film resistor

L1 to L7 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100A or capacitor of same quality.



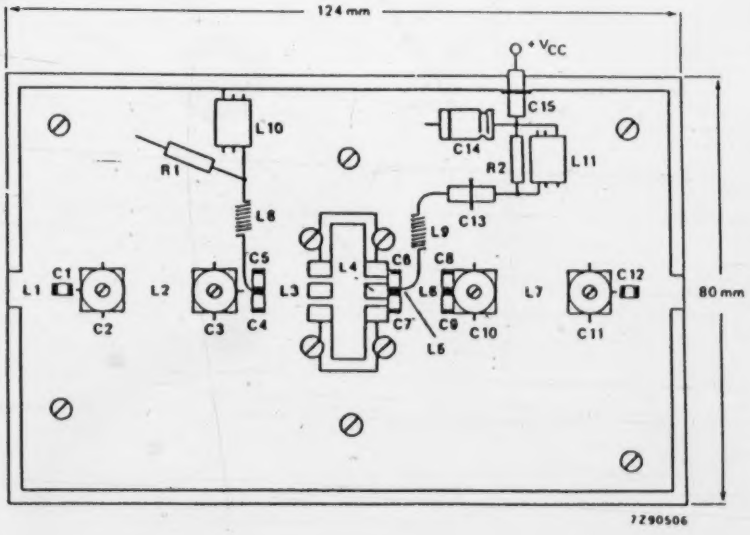


Fig. 8 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of the P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by fixing screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

RUGGEDNESS

The device is capable of withstanding a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V and at T_h = 25 °C.

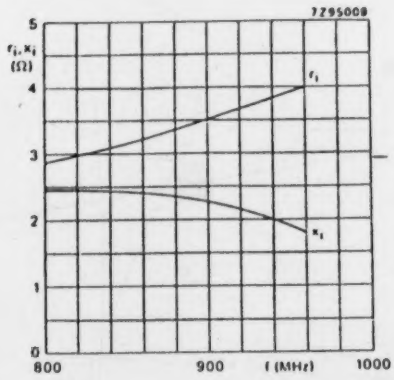


Fig. 13 Input impedance (series components).

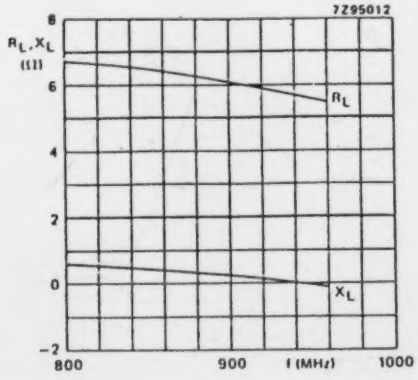


Fig. 14 Load impedance (series components).

Conditions for Figs 13 and 14:

V_{CE} = 12,5 V; P_L = 8 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

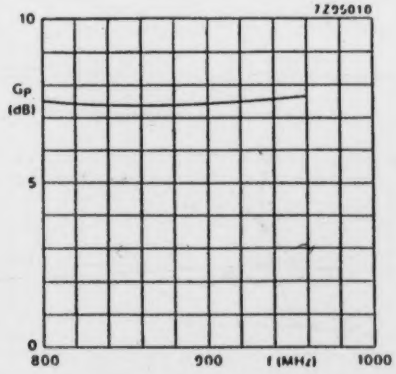


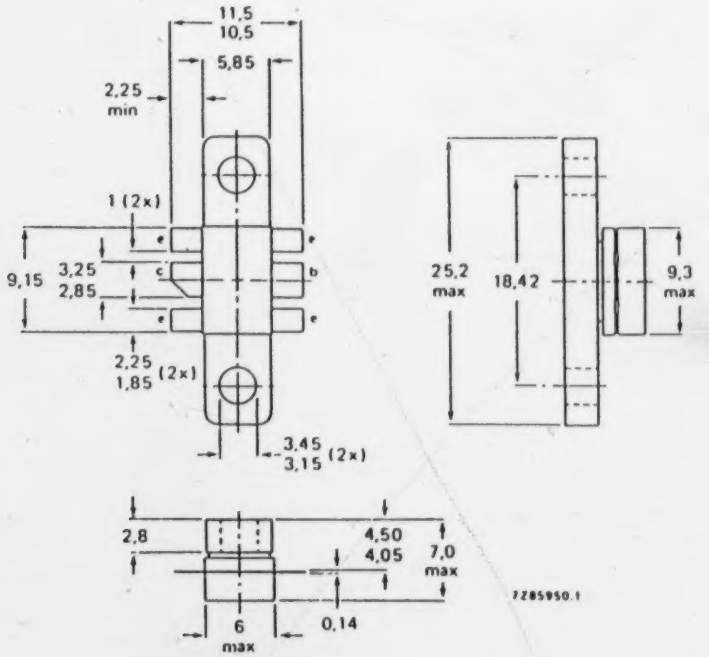
Fig. 15 Power gain vs. frequency.

V_{CE} = 12,5 V; P_L = 8 W; f = 800–960 MHz; T_h = 25 °C; class-B operation; typical values.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-171.



Torque on screw: min. 0,6 Nm (6 kg.cm)
max. 0,75 Nm (7,5 kg.cm)

Recommended screw: cheese-head 4-40 UNC/2A

Heatsink compound must be applied sparingly and evenly distributed.

APPENDIX B

C/NL* Analysis and Optimization Program

General Description

* C/NL Version II.2

Nonlinear Consulting
P.O. Box 7284
Long Beach, CA, U.S.A.
90807

C/NL is an analysis and optimization program for linear RF and microwave circuits. Gain, return loss, and noise performance can be analyzed with the program. The C/NL program also provides non-linear distortion analysis using Volterra series.

All functions provided by the C/NL program are accessed via its menu-driven user interface. Circuits are entered into ASCII data files, which are read by the program when an analysis is requested (the format is similar to a SPICE deck). The data file also contains the desired analysis and/or optimization options.

C/NL provides three optimizers: a proprietary random optimizer, a Fletcher/Reeves conjugate-gradient optimizer, and a Nelder/Meade downhill simplex optimizer. These algorithms are used to minimize the error function, err:

$$err = \frac{1}{N} \sum_{n=1}^{N} \sum_{i=1}^{2} \sum_{j=1}^{2} W|S_{ij}| \left(|S_{ij(c)}| - |S_{ij(m)}|\right)^2 + W_{<}S_{ij} \left(<S_{ij(c)} - <S_{ij(m)}\right)^2$$
$$+ WNF \left(NF_{(c)} - NF_{(m)}\right)^2 + WIP \left(IP_{(c)} - IP_{(m)}\right)^2$$

where W__ are the user-defined weighting values for each of the error terms

(m) denotes the measured or target value of a specific parameter

(c) denotes the calculated value of a specific parameter

Each of the optimizers provides a unique combination of performance and efficiency. For example, the random optimizer requires the least number of functional evaluations per iteration. However, the final results may not represent the optimal solution. The other optimizers are less efficient and require a relatively long initialization process. These are better at finishing the optimization process, after the random optimizer has stopped. The most

efficient optimization method is to use the random optimizer to locate the initial minimum, and then to use one of the other optimizers to complete the process.

In addition to the analysis and optimization functions, C/NL provides several utilities for converting the results to the desired parameter set, calculating stability circles, and generating plots of the results (linear or Smith Chart plots).

APPENDIX C

PSpice Input File for Simulating the

Experimental Class B Amplifier

```
******* 05/23/91 ******* Evaluation PSpice (July 1989) ******* 18:47:48 ******

blv93sim

****     CIRCUIT DESCRIPTION

**********************************************************************



*SPICE_NET
*
.TRAN 0.05NS 450NS 400NS
.OPTIONS ITL5=0
.MODEL BLV93 NPN(IS=1.2E-14 NE=1.4 BF=75 ISE=2.56E-13 VAF=78
+              RC=.25 RE=0.1 RB=1.4 BR=7 NC=1.12
+              CJE=70PF VJE=0.57 MJE=0.52 XTB=1.5
+              CJC=29PF VJC=0.47 MJC=0.59 TF=50PS)
*
* source and input network
*
VG 1 0 SIN 0 29 850MEG
RS 1 2 50
CTRANS1 2 0 0.082PF
LTRANS1 2 3 0.103NH
T1 3 0 4 0 Z0=49.2 F=860MEG NL=0.946
C1 4 5 33PF
C23 5 0 10.91PF
T2 5 0 6 0 Z0=45.6 F=860MEG NL=0.124
C34 6 0 3.8PF
T3 6 0 7 0 Z0=51.04 F=860MEG NL=0.026
C67 7 0 12.59PF
L1 7 70 45NH
L2 70 0 45NH
C2 70 0 0.001UF
R1 70 0 10
T4 7 0 8 0 Z0=42.91 F=860MEG NL=0.0583
*
* output network and load
*
T5 9 0 10 0 Z0=56.49 F=860MEG NL=0.0278
C89 10 0 14.73PF
L3 10 11 245NH
L4 11 111 100NH
C18 111 0 150PF
R2 11 111 10
VCC 111 0 12.5
T6 10 0 12 0 Z0=42.12 F=860MEG NL=0.019
T7 12 0 13 0 Z0=62.04 F=860MEG NL=0.0454
C10 13 0 14.14PF
```

```
T8 13 0 14 0 Z0=41.1 F=860MEG NL=0.152
C14 14 0 9.81PF
C16 14 144 33PF
T9 144 0 15 0 Z0=63.68 F=860MEG NL=0.0485
LTRANS2 15 16 0.1336NH
CTRANS2 16 0 0.098PF
RL 16 0 50
*
* transistor and emitter inductance
*
LP1 8 50 0.65NH
CP1 50 0 75PF
LP2 50 51 0.38NH
CP2 51 52 6.5PF
LP3 52 9 0.003NH
CP3 52 0 1.0PF
Q1 52 51 0 BLV93
*
.PROBE
*.TEMP 66.2
.END
```